

Internal Scan Test Methodology of Sequential Circuits

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ABSTRACT

Semiconductor industries goal for the quality of products is to satisfy customer requirements. Higher quantity of electronic devices can only be obtained by scan tests of the manufactured components. Scan chains are universally used in large industrial designs in order to cost effective test manufactured electronic devices. Yet, faults in the scan cells are not directly targeted by the existing tests. The main objective of this paper is to investigate the testability of the faults internal to scan cells (Sequential circuits). The major difficulty in sequential circuit testing is in determining the internal state of the circuit. Scan design techniques are directed at improving the controllability and Observability of the internal states. The approach aims to reduce the problem of testing a sequential circuit to that of testing combinational logic.

Keywords: DFT, ATPG, ITG, D Flip-Flop, LSSD.

I. INTRODUCTION

This technique is used to detect defects in digital ICs and PC board systems. The goal of testing is to apply a minimum set of input vectors to each device to determine if it contains a defect. The first step is to detect defects at the manufacturing level at the earliest point possible. Costs increase dramatically as faulty components find their way into higher levels of integration. A relationship known as “the rule of ten” is applied for test cost.

\$1.00 to fix an IC (throw it out) \$10.00 to find and replace bad IC on a PC board \$100.00 to find bad PC board in a system \$1000.00 to find bad component in fielded system
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System Partitioning: System is partitioned into subsystem and provides special test point at the interface of the subsystem. For example, a finite state machine has n input and m memory elements for this system 2^{m+n}

test vector required. If we partitioned then only $2^m + 2^n$ test vector required.

Design for testability (DFT) makes it possible to: Assure the detection of all faults in a circuit reduce the cost and time associated with test development. Reduce the execution time of performing test on fabricated chips.

There are two key concepts for testability.

1. Controllability
2. Observability

Controllability: ease of forcing a node to 0 or 1 by driving input of the chip.

Observability: ease of observing a node by watching external output pins of the chip.

Good Observability and controllability reduces number of test vectors required for manufacturing test.

- Reduces the cost of testing
- Motivate design-for-test.

Combinational logic is usually easy to observe and control. Finite state machines can be very difficult, requiring many cycles to enter desired state- especially if state transition diagram is not known to the test engineer.

II. TESTING SEQUENTIAL LOGIC

Sequential circuits may be generally represented as finite state machines, may be modeled as combinational logic with a set of delays and feedback from output to input as shown in figure (1).

The ‘ m ’ feedback variables constitute the state vector and determine the maximum number of finite states which may be assumed by the circuit. In the most general cases, the next state and the output are both functions of the present state and the independent inputs. The delay elements are generally assumed to be associated with the feedback path and, for clocked systems, the basic delay elements are flip-flops.

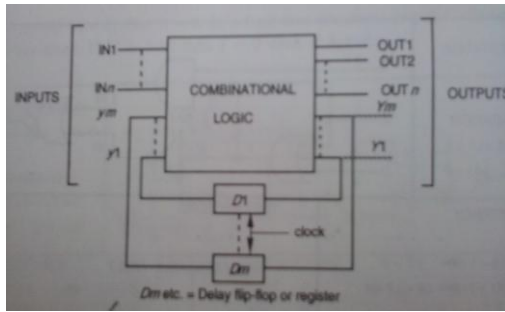


Figure (1): Sequential logic testing- Finite state machine model

(a) The Scan Path

A sequential circuit comprises combinational logic and storage elements- usually in the feedback path- as illustrated in figure (2). Scan path design techniques configure the logic so that the inputs and outputs of the combinational part can be accessed and storage elements reconfigured to form a shift register known as the scan path. Thus the internal states of the circuit can be observed and controlled by shifting (scanning) out the contents of the storage elements.

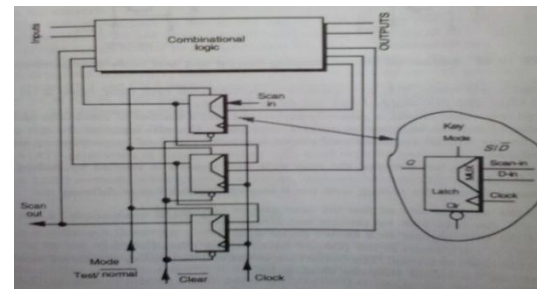


Figure (2): Sequential circuit configured for scan path testing.

The test generation for a sequential circuit is a very complicated task since the test signals must not only be logically correct but must also occur at the correct time relative to other signals. All sequential circuits exhibit a memory property since, in deciding what to do next, it is not only the test pattern but also the order or sequence in which it is applied is significant.

III. THE ITERATIVE TEST GENERATION METHOD

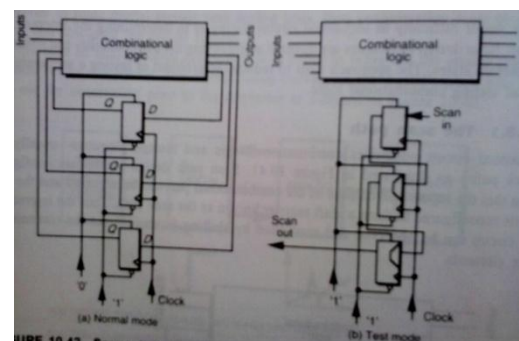
A way of approaching the testing of sequential logic is to ‘convert’ the logic into combinational logic by cutting the feedback lines. For an N-state machine, this arrangement is then replicated N times so that an N-state sequential machine is converted into an N-time frame combinational machine.

The main problem of this technique is that a simple fault in the sequential machine is manifest as N multiple faults during test. This is time-consuming for circuit of any complexity. It is also necessary to describe all the initial states of the circuit, which is also time-consuming. For these reasons the iterative test generation (ITG) methods are best suited to logic with few feedback loops as in control logic for example.

The storage elements are usually ‘D’, ‘JK’ or ‘RS’ flip-flop elements with the classical structure being modified by the addition of a two-way multiplexer on the data input(s). The multiplexer is controlled by an external “mode” signal and allows the scan path reconfiguration to be effected. In figures (2) and (3) a basic ‘D’ flip-flop has been shown with the added input multiplexer. This configuration is commonly known as an ‘MD’ (multiplexed ‘D’) flip-flop. The sequential circuit containing the scan path has two modes of operation- a normal and a test mode. The configuration associated with each basic mode is set out in figure (3) (a) and (b) normal and test mode respectively.

IV. SCAN DESIGN TECHNIQUES

The scan design techniques which are now to be discussed are structured approaches to designing sequential circuits so that testability is ‘designed in’ from the outset. The major difficulty in sequential circuit testing is in determining the internal state of the circuit. Scan design techniques are directed at improving the controllability and Observability of the internal states. The approach aims to reduce the problem of testing a sequential circuit to that of testing combinational logic.



(a) Normal mode (b) Test mode

Figure (3): Sequential circuit showing normal and test mode configurations.

A large sequential circuit is generally partitioned into a number of sub-circuits each with a combinational section and one associated scan path. The efficiency of the test pattern generation for the overall combinational circuit is greatly improved by partitioning since its depth is reduced. Before applying test patterns, the scan path shift register is verified by shifting in all ones then all zeroes.

(b) Testing Steps With Scan Path

General steps for testing with the scan path approach are as follows:

1. Set the mode to *test* so that the scan path is configured.
2. Verify the scan path by shifting test data in and out.
3. Set the shift register to a known initial state.
4. Apply a test pattern to the primary inputs of the overall circuit.
5. Set the mode to *normal*. The circuit then settles and the primary outputs are monitored.
6. Activate the circuit with one clock pulse.
7. Return to the test mode.
8. Scan out the contents of the scan path registers and simultaneously scan in the next pattern.
9. Repeat from step (4) etc.

(c) Level-Sensitive Scan Design (LSSD)

LSSD Design Rules:

- Rule 1: Use hazard-free polarity-hold latches.
- Rule 2: Latches are controlled by two non- overlapping clocks such that:

- a) One feeds the other, cannot have the same clock
- b) Gated clock by latch X cannot clock latch X

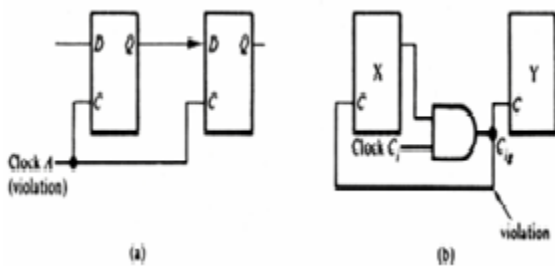


Figure (4)

Rule 3:

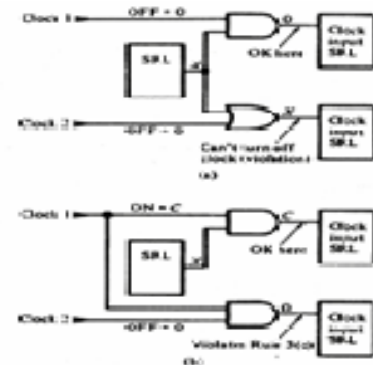


Figure (5)

Rule 4: Clock primary inputs may not feed the data inputs to latches.

Rule 5: All SRLs must be interconnected into one or more shift registers

Rule 6: Sensitizing condition (Shifting)

Advantages of the LSSD Technique

1. The correct operation of the logic network is independent of characteristics such as clock edge rise time and fall time.
2. Network is combinational in nature as far as test generation and testing is concerned.
3. The elimination of all hazards and races greatly simplifies both test generation and fault simulation.

V. CONCLUSION

With the advent of nanometer technologies the design size of ICs is getting larger and the operation speed is getting faster. As a consequence, test cost is becoming unbearable with traditional methods.

The big challenge for the design and test engineers is how to guarantee the required high level of test quality and yield while keeping the test cost low.

From a scan based ATPG point of view there are two main ways to reduce test cost. First is to reduce the test pattern volume and test run time which is not possible with the quality of testing. The other way is to use lower end tester, which are much cheaper but have limited memory, data channels and clocking capabilities. Internal scan test is a quite good method for testing but it also has its limitations like slow speed and large data volume.

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