Analyzing Aliasing effect in Down Sampler with increase in factor M

[1]Monica Singhal, [2]Rajesh Mehra
[1]M.E Scholar, NITTTR, Chandigarh, India
[2]Associate Professor, NITTTR, Chandigarh, India

ABSTRACT

This paper presents the analysis of aliasing effects in various signals due to down sampling. Decimation is used for decreasing the sampling rate. Aliasing is an effect that causes original signal to degrade its shape due to down sampling. The aliasing effect is analyzed on Sinc, Sine, Saw tooth and Square signals by taking three different down sampling factor M samples using MATLAB. The simulator result shows that if Nyquist criteria are not followed during down sampling then signal loses its shape that degrades the system performance. The Aliasing effect is less in case of Sinc signal as compared to other three signals.

Key Words: DSP, Decimator, FIR, Multirate , TDM

I. INTRODUCTION

DSP is the mathematical manipulation of an information signal to modify or to improve it. It is characterized by the representation of discrete time, discrete frequency, or other discrete domain signals by a sequence of numbers or symbols and the processing of these signals. Digital processing allows the sharing of a given processor among the number of signals by timesharing, thus reduces the cost of processing per signal. In timesharing, signals are combined by time-division multiplexing (TDM). The multiplexed signals can fed into a single processor. By switching the processor coefficients on the arrival of each signal at the input of the processor, the processor made to look like two different systems. Finally, at the output of the processor, processed signal can be separated by time division demultiplexing [1].

Digital processing of an analog signal is carried out in three steps: conversion of signal into discrete form, processing of digital signal, and finally conversion of processed digital signal into analog form at the output. The amplitude of the analog signal is time dependent. Sample and hold circuit provide analog signal at periodic time intervals and hold the sampled values at analog to digital converter output. The digital output is then processed by digital processors implementing the digital signal processing algorithm. The output of the processor is then converted into staircase-type analog input by digital-to-analog converter (ADC). Some of the advantages of DSP are Digital implementation permits easy adjustment of the processor characteristics during processing. Such adjustments can be simply carried out by periodically changing the coefficients of the algorithm representing the processor characteristics [1].

Filter is a frequency selective circuit that allows a certain band of frequency to pass while attenuating the others frequencies. Filters are classified as analog and digital. The Digital Filtering is one of the most powerful tools of DSP. The input and output signals in the digital filter is digital or discrete time variant [2]. For designing the digital filters, first determine set of filter coefficients to meet design specifications. Digital filters are of two types: FIR and IIR. In digital filtering, linear transformation of the samples surrounding the current samples takes place. Digital filters are useful in digital signal processing applications, signal analysis and estimation of signals. In filters, by varying the weight of the coefficients and filter taps, frequency response characteristics can be realized with an FIR filter. FIR filters exhibit linear phase shift for all frequencies. FIR filters are filters having a transfer function of a polynomial in z-plane and is an all-zero filter in the sense that the zeroes in the z-plane determine the frequency response magnitude characteristic [3, 4]. The z transform of a N-point FIR filter is given by

$$h(z) = \sum_{n=0}^{N-1} h(n)z^{-n} \qquad (1)$$

IIR filters have infinite impulse response. In IIR filters their phase characteristics is not linear, which can cause a problem to the systems which need phase linearity [2]. The sampling rate conversion leads to the production of unwanted signals associated with aliasing. Some type of filters should be placed in order to attenuate these errors. There are some sampling rate alternating devices along with Conventional elements such as an adder, multiplier, and a delay. Discrete time systems which

provide unequal sampling rates at various positions are called multi rate systems. The function of multi rate system is to alter the position of the discrete signals, by deleting some of the signal samples [3].They are useful in various signal processing techniques such as analysis, reducing noise, compression, analog to digital converter, etc.

Multirate signal processing is used to introduce some redundant bits in the data at the transmitter side. Redundancy is added to avoid noise amplification and to offer flexibility for symbol synchronization at the receiver. The digital signal processing reduces the need of anti-aliasing filter, which leads reduction in cost and power. The multirate DSP also provide additional degrees of freedom in the design of the receiver in communication system. Various advantages of Multirate DSP are less storage for filter coefficient, low order is required, less sensitive to filter coefficient [5, 6].

II. DOWN SAMPLING

In multi rate system, system parts operate at different sampling frequencies and they must perform signal rate conversion between these parts. This can be done by interpolation which increases the sampling frequency or by decimation which decrease the sampling frequency of the signal. In signal rate conversion take place, first by constructing the corresponding analog signal and then, resample with new sampling frequency. Sampling frequency change can result in low implementation cost as the arithmetic operations, i.e., additions and multiplications can be performed at a lower rate. Down samplers are required in Decimation [3, 7].
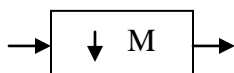

Figure 1: Down sampler

For decimation low pass filters are used. When decimation is done bandwidth of a signal is reduced to an appropriates level so that minimal aliasing occurs. Down sampler for a factor M is achieved by discarding every M-1 samples or by keeping every Mth sample. While discarding M-1 sample for every M samples the original sample rate is reduced by a factor of M. To remove this effect, the signal must be low pass filtered to remove frequency components from the output spectrum which is required to be alias free. The benefit

of decimation is that the low pass filter may be operated to design at the decimated sample rate, rather than the input sample rate by using an FIR filter [4].

Let $x(n)$ be the input signal, $h(k)$, $0 \leq k \leq M$ be the coefficients of a low pass filter and $z(n)$ be the output signal before decimating by factor M [8]. The output signal after the decimator be

$$y(n)=z(nM) \tag{2}$$

Apply z-transform to the input-output relation of a factor-of-M down-sampler, we get

$$Y(z)=\sum_{n=-\infty}^{n=\infty} x[nM]\,z^{-n} \tag{3}$$

The expression on the right-hand side of Eq (3) cannot be directly expressed in terms of X(z). To get away from this problem, a new sequence $x_{int}\,[n]$ can be expressed as:

$$x_{int}\,[n]= \begin{cases} x[n] & 0, \pm M, \pm 2M, \ldots\ldots. \\ 0 & \text{otherwise} \end{cases} \tag{4}$$

Then

$$Y(z) = \sum_{n=-\infty}^{n=\infty} x[nM]\,z^{-n}$$
$$= \sum_{n=-\infty}^{n=\infty} x_{int}\,[nM]\,z^{-n}$$
$$\sum_{k=-\infty}^{k=\infty} x_{int}\,[k]\,z^{-k/M} = x_{int}\,[z^{1/M}] \tag{5}$$

Now, $x_{int}\,[n]$ can be formally related to $x[n]$ as
$$x_{int}\,[n]=c[n]x[n] \tag{6}$$

Where

$$c[n]= \begin{cases} 1 & 0, \pm M, \pm 2M \\ 0 & \text{otherwise} \end{cases} \tag{7}$$

The representation of c[n] is given by

$$c[n]= \frac{1}{M}\sum_{k=0}^{k=M-1} W_M^{kn} \tag{8}$$

Making use of Eq. (8) in the z transform of $x_{int}\,[n]$, we get [1]

$$\boldsymbol{X_{int}[n]} = \sum_{n=-\infty}^{n=\infty} \boldsymbol{c[n]x[n]\,z^{-n}}$$
$$= \frac{1}{M}\sum_{n=-\infty}^{n=\infty} \left(\sum_{k=0}^{M-1} W_M^{kn}\right)x[n]z^{-n}$$
$$= \frac{1}{M}\sum_{k=0}^{M-1} \left(\sum_{n=-\infty}^{\infty} W_M^{kn}\,x[n]z^{-n}\right)$$
$$= \frac{1}{M}\sum_{k=0}^{M-1} X(zW_M^{-k}) \tag{9}$$

The desired input-output relation in the transform domain for the factor of M down sampler is then obtained by substituting Eq. (9) in Eq. (5)

$$Y(z) = \frac{1}{M}\sum_{k=0}^{M-1} X(z^{1/M}W_M^{-k}) \qquad (10)$$

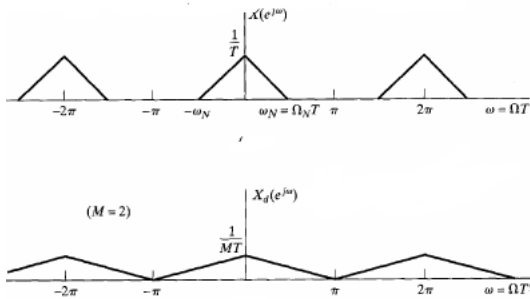The spectrum of a factor-of-2 down-sampler [4] with an input x[n] is shown in Fig 2.

Figure 2: Spectrum of down sampler

The DTFTs of the output and the input sequences of this down-sampler are then related as

$$Y(e^{jw}) = \frac{1}{2}[X(e^{jw/2}) + X(e^{-jw/2})] \qquad (11)$$

The second term in above equation is simply obtained by shifting the first term $X(e^{jw/2})$ to the right by an Amount 2π as shown in Fig 3. The two terms have an overlap due to which original "*shape*" of $X(e^{jw/2})$ is lost when *x*[*n*] is down-sampled. This overlap causes the *aliasing* that takes place due to under-sampling [4]. There is no overlap, i.e., no aliasing, only if

$$X(e^{jw/2}) = 0 \qquad \text{for } |w| \geq \frac{\Pi}{M} \qquad (12)$$
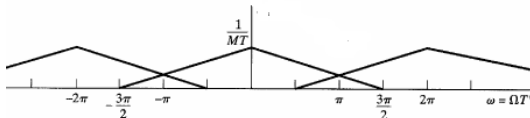
Figure 3: Aliasing effect

To overcome the effect of aliasing decimation filters are used. The specifications for the low pass decimation filter are given by [3]

$$|H(e^{jw})| = \begin{cases} 1 & |w| \leq w_c/M \\ 0 & \Pi/M \leq |w| \leq \Pi \end{cases} \qquad (13)$$

3. MALTAB BASED DESIGN

Figure 4 shows down sampling of Sinc signal with down sampling factor M=2. The output signal provides the complete information as it free from aliasing effect. No Aliasing effect is present as it follows the Nyquist criteria.
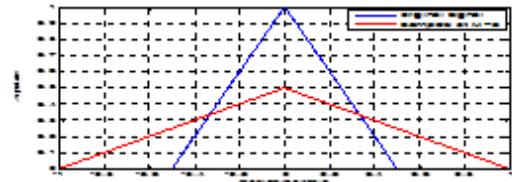

Figure 4: Frequency domain representation

Figure 5 shows down sampling of Sinc signal with M=5. The output signal deviates from its original signal due to down sampling. By increasing the M, the aliasing effect increases.
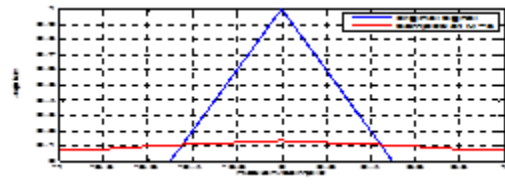

Figure 5: Frequency domain representation

Figure 6 shows that when Sinc signal is down sampled by M=10, a constant signal is obtained. This shows that aliasing effect causes original shape to lose its shape
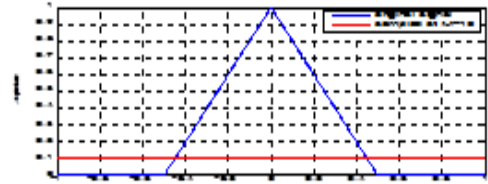

Figure 6: Frequency domain representation

Figure 7-9 shows down sampling of Sine signal with down sampling factor M=2, M=5 and M=10. Down Sampling causes M-1 samples to be discarded causing sampling rate to be reduced by M factor. Thus reduction in sampling rate causes aliasing effect as M-1 samples are discarded.
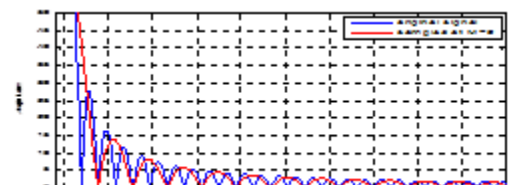

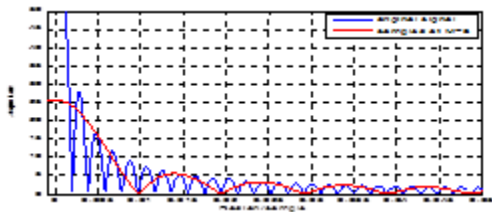Figure 7: Frequency domain representation

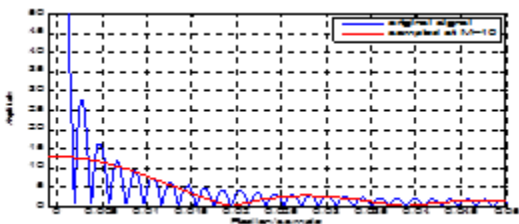Figure 8: Frequency domain representation

Figure 9: Frequency domain representation

Figure 10-12 shows aliasing effect in Square signal with down sampling factor M=2, M=5 and M=10. From the figures it is clear that the aliasing effect increases with increase in M. As M increases the signal deviates more from its original shape as M-1 samples are discarded.
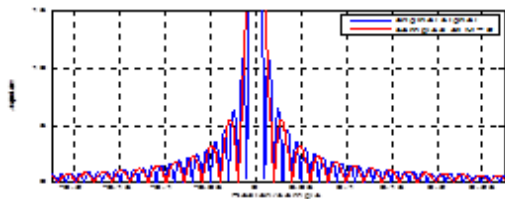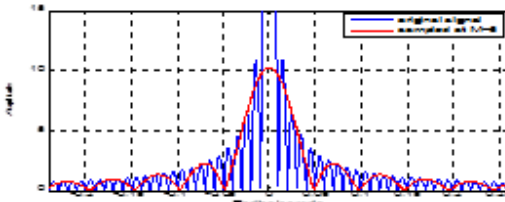

Figure 10: Frequency domain representation
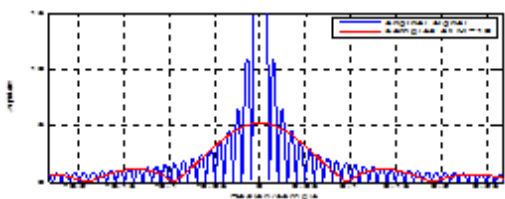

Figure 11: Frequency domain representation

Figure 12: Frequency domain representation

Down sampling of Sawtooth signal for down sampling factor M=2, M=5, M=10 is shown in figure 13-15.The frequency domain representation of signals with

different M shows increase in aliasing effect. Output signal discard M-1 samples thus reducing sampling rate.
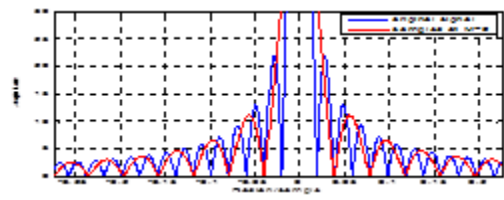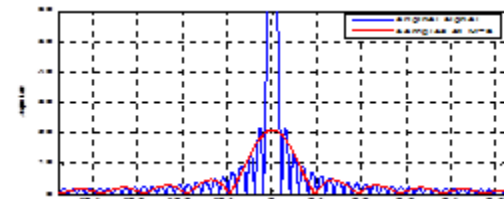

Figure 13: Frequency domain representation
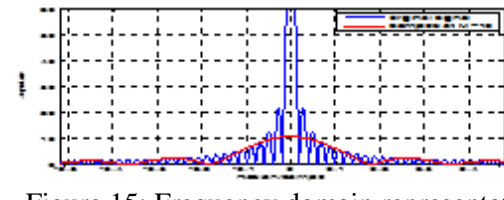

Figure 14: Frequency domain representation

Figure 15: Frequency domain representation

IV. COMPARATIVE ANALYSIS

Down sampling for four different signals are analyzed using three down sampling factor M (2, 5, and 10). The frequency domain representation of four different signals shows that the aliasing effect increases with increase in M factor. Increase in M causes signal to lose its original shape.
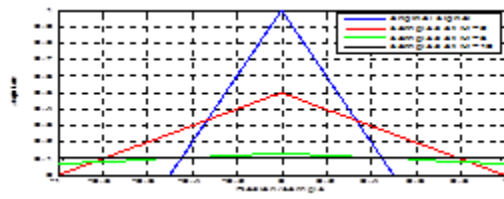

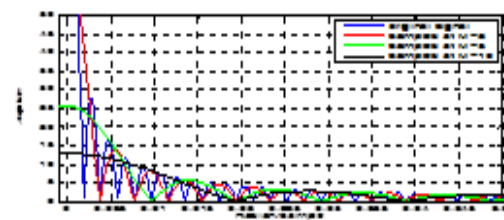Figure 16: Frequency domain representation

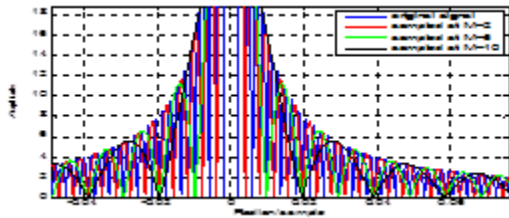Figure 17: Frequency domain representation
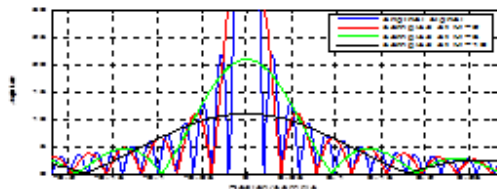
Figure 18: Frequency domain representation

Figure 19: Frequency domain representation

Figure 16-19 shows frequency domain representation of Sinc, Sine, Square and Sawtooth signal. From the above results it is observed that increase in M causes more deviation from the original signal. Deviation results in aliasing effect. Down sampling discard M-1 samples from each signal thus sampling rate is reduce by factor M. But sinc signal show zero aliasing at M=2 as compare to other signals.

V. CONCLUSION

It is observed that, as down sampling factor M increases the aliasing effect increases in all four different signals (Sinc, Sine, Square and Sawtooth). Four different signals show different aliasing effect with different M. Among the four signals sinc signal show no aliasing for M=2. In all signals aliasing is increasing with increase in M. Aliasing effect deviates the original signal and it loose its original shape. Aliasing effect occurs as M-1 samples are discarded from M samples. Signal loses its original shape and samples are lost due to aliasing.

REFERENCES
[1] Sanjit K Mitra, "Digital Signal Processing", Tata Mc Graw Hill, Third Edition, pp 36-39,745-747, 2010.

[2] Sonika Gupta ,Aman Panchal, "Performance analysis of FIR filter design by using rectangular, hanning and hamming windows method", International Journal of advanced research in Computer science and Software Engineering, Vol. 2, Issue 5, pp 273-277, June-2012.

[3] Rajesh Mehra, Swapna devi, "Optimized design for Decimator for alias removal in multirate DSP application", International Conference on Engineering Mechanics, Structure, pp 100-103.

[4] S Salivahanan, Digital signal processing,. Tata Mc Graw Hill, Third Edition, pp 526-529, 2006.

[5] John G. Proakis, Dimitris G. Manolakis, "Digital Signal Processing: Principles, Algorithms, and Applications", Pearson Education, Fourth Edition, pp. 740-749, 2008.

[6].Yonghao Wang and Joshua Reiss," Time domain performance of decimation filter architectures for high resolution sigma", pp 8648-8652, April-2012.

[7] ShyhJye Jou, Kai-Yuan Jheng*, Hsiao-Yun Chen and An-Yeu Wu, "Multiplier less Multirate Decimator Interpolator Module Generator", IEEE Asia-Pacific Conference on Advanced System Integrated Circuits, pp. 58-61, Aug-2004.

[8] Shang-Chen Wu and Masayoshi Tomizuka, "Performance and Aliasing Analysis of Multi-rate Digital Controllers with Interlacing", America control conference Boston , pp 3514-3519, June-2004.

AUTHORS

Monica Singhal received the Bachelors of Technology degree in Electronics and Communication Engineering from Bharat Institute of technology, Meerut India in 2010, and Perusing Masters of Engineering degree in Electronics and Communication Engineering from National Institute of Technical Teachers' Training & Research, Punjab University, Chandigarh, India. She is an Assistant Professor in the Department of Electronics & Communication Engineering,, Meerut Institute of Engineering and Technology, Meerut, India. Her teaching interests are in Digital signal design,

Rajesh Mehra received the Bachelors of Technology degree in Electronics and Communication Engineering from National Institute of Technology, Jalandhar, India in 1994, and the

Masters of Engineering degree in Electronics and Communication Engineering from National Institute of Technical Teachers' Training & Research, Panjab Unibersity, Chandigarh, India in 2008. He is pursuing Doctor of Philosophy degree in Electronics and Communication Engineering from National Institute of Technical Teachers' Training & Research, Punjab University, Chandigarh, India.

He is an Associate Professor with the Department of Electronics & Communication Engineering,, National Institute of Technical Teachers' Training & Research, Ministry of Human Resource Development, Chandigarh, India. His current research and teaching interests are in Signal, and Communications Processing, Very Large Scale Integration Design. He has authored more than 175 research publications including more than 100 in Journals. Mr. Mehra is member of IEEE and ISTE.