Design of 32nm CMOS EIS Comparator for N-Bit Flash ADC

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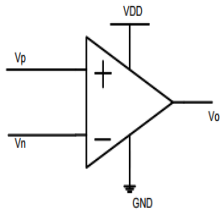
Abstract
The design methods and optimization of the 32nm CMOS EIS (Efficient Inverter scheme) comparator circuit for an N bit flash A/D converter are presented in this paper. Flash A/D converter requires 2^n-1 comparators. Each one different from all others depends on the particular design. The used analog power supply in this comparator is only 1V. Low voltage analog design is necessary to compile so As to get decreasing digital supply voltage used for the complete mixed-signal chip. Supply voltages in deep submicron CMOS technologies decrease due to the short channel effects and decrease with the technology length. Optimal design method of the EIS comparator presented in this paper significantly improves the linearity of the A/D converter against the CMOS process variation.

Keyword: *32nm, CMOS, EIS, Flash A/Ds, PTM, LT-Spice*

1-Introduction
A flash Analog to Digital Converter (ADC) architecture is mainly used for its high-speed conversion rate application. Flash A/D consumes more power and occupies larger chip area in comparison to the other types of A/DCs, such as pipelined and Successive Approximation ADCs. The latest VLSI design trend for signal processing system demands high-speed and low power consumption. In this paper, the authors present an optimal design method of the CMOS EIS comparators. The resulting flash ADC features higher speed, lower power consumption, smaller size, and more readiness for the SOC integration.

2-CMOS EIS Comparator
CMOS EIS Comparator is also known as Complementary Metal Oxide Semiconductor FET Efficient Inverter Scheme (EIS) Comparator. These comparators are very efficient in power consumption and dissipate the power in micro watt range.

Comparator is a circuit that detect whether a signal is greater or smaller than reference signal.



$V_P < V_N$ then V_O = VSS= logic 0.

$V_P > V_N$ then V_O = VDD= logic 1.

Figure-1 Comparator operation

The block diagram of comparator is shown in figure-1. If the +ve, V_P, the input of the comparator is at a greater potential than the -ve, V_N, input, the output of the comparator is a logic 1, where as if the + input is at a potential less than the –input, the output of the comparator is at logic 0. Below figure-2 shows the efficient inverter scheme based TIQ CMOS comparator.

2.1-CMOS Inverter as a Comparator
The inverter threshold voltage Vm is defined as the Vin = Vout point in the VTC of an inverter. Mathematically,

$$V_m = \frac{r\left(V_{DD} - \left|V_{Tp}\right|\right) + V_{Tn}}{1+r} \quad \text{with} \quad r = \sqrt{\frac{k_p}{k_n}}$$

where V_{Tp} and V_{Tn} represent the threshold voltages of the PMOS and NMOS devices, respectively.

2.2-TIQ Comparator
Commonly used comparator structures in CMOS ADC design are the fully differential latch comparator and the dynamic comparator. The former is sometimes called a clocked comparator, and the latter is called an auto-zero comparator or chopper comparator. To achieve high speed, such comparators are usually implemented with bipolar transistor technology. For SoC implementation in this case, BiCMOS technology would be necessary to integrate both a high-speed ADC and a digital signal process on the same substrate. The TIQ(Threshold

Inverter Quantization) comparator used two cascaded Complementary MOS inverters as a comparator for high speed conversion application and low-power dissipation. The proposed TIQ comparator that is described in this paper has been developed not only for higher speed but also for higher resolution. Implemented flash Analog to digital converter based on the Threshold Inverter Quantization (TIQ) technique for its high speed and low power using standard CMOS technology. Some of the basic problems of the conventional comparators circuit used in Analog to digital converter designs are:

i) Large transistor area,
ii) Charge injection errors,
iii) DC bias requirement,
iv) Metastability errors,
v) High power consumption,
vi) capacitor or Resistor array requirement.

Such type of problems can be reduced by using Threshold Inverter Quantization. The TIQ technique has many advantages, viz;

i)Less complecated simpler voltage comparator circuit,
ii) fastest voltage comparison speed,
iii) eliminates of resistor ladder circuit,
iv) does not require clock signal, switches, or coupling Capacitors for the voltage comparison. This design technique is done such that the comparator consumes minimum power even at a very high speed conversion rate.

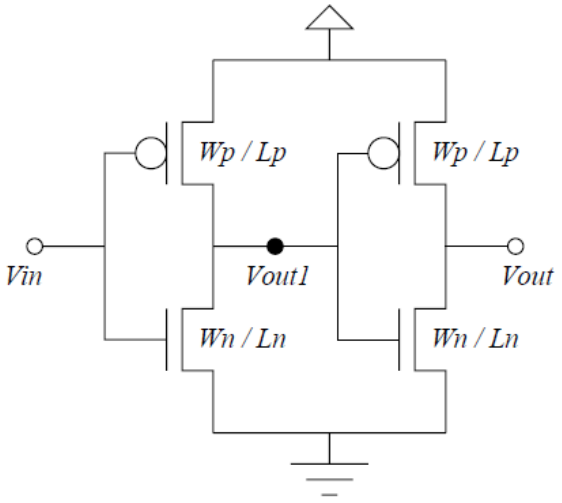


Figure-2 The schematic of the TIQ comparator

Figure-2 shows the schematic of the TIQ comparator and figure-3 it's VTC from the simulation. At the first inverter, the analog input signal quantization level is set by Vm, depending on the W/L ratios of PMOS and NMOS. The second inverter is used to increase voltage gain and to prevent an unbalanced propagation delay. In Figure 3, the slope of Vout is shown larger than that of Vout1. The inverter threshold depends on the transistor sizes. The C1 and C2 curves show the difference in the VTC of Vout.

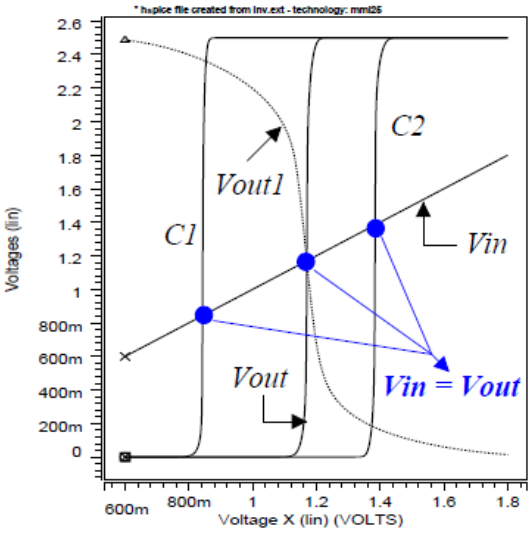


Figure-3 VTC of the TIQ comparator

With a fixed length of the PMOS and NMOS devices, we can get desired values of C1 and C2 by increasing only the width of the PMOS and NMOS transistors, respectively. This result can be confirmed by the following equation of the inverter threshold.

$$V_m = \frac{\sqrt{\frac{\mu_p W_p}{\mu_n W_n}}\left(V_{DD} - \left|V_{Tp}\right|\right) + V_{Tn}}{1 + \sqrt{\frac{\mu_p W_p}{\mu_n W_n}}}$$

where $\boldsymbol{\mu}_p$ and $\boldsymbol{\mu}_n$ are the electron and hole mobility, respectively. To derive this Equation
we assume that both transistors are in the active region, the gate oxide thickness (Cox) for both transistors is the same, and the lengths of both transistors (Lp and Ln) are also the same. From this Equation we know that Vm is shifted, depending on the transistor width ratio (Wp/Wn). That is, increasing Wp makes Vm larger, and increasing Wn makes Vm smaller on the VTC. This changing of the widths of the PMOS and NMOS devices with a fixed transistor length is the idea of the TIQ comparator. We can use the inverter threshold
voltage as an internal reference voltage to compare the input voltage. However, to use the CMOS inverter as a voltage comparator, we should check the sensitivity of Vm to other parameters, which are ignored in Equation this, for correct operation of the TIQ flash ADC. In a mixed-signal design, the ignored parameters - threshold

voltages of both transistors, electron and hole mobility, and power supply voltage - are not fixed at a constant value. The following sections will discuss the TIQ flash ADC sensitivity to process, temperature, and power supply voltage.

i. Sensitivity to Process

For implementing the TIQ comparator,PTM Low Power 32nm Metal Gate / High-K / Strained-Si, is used. We cannot be sure that the
simulation results with this MOS transistor model will be exactly matched with the measurement results. Therefore, we need a more complete transistor model for the inverter threshold sensitivity to reduce the gap between the simulation results and the measurement results. Moreover, if we apply another transistor model that was not used in our ADC design, the inverter threshold sensitivity will be critical in the TIQ comparator. Since process parameters change from one fabrication to another, the inverter threshold voltage will change. This situation is one of major problems for linearity errors of the TIQ comparator which uses Vm as a reference voltage.

ii. Sensitivity to Temperature

The inverter threshold voltage also depends on temperature according to the following partial differential equation.

$$\frac{\partial V_m}{\partial T} = \frac{1}{1+\sqrt{\frac{\mu_p W_p}{\mu_n W_n}}} \left(\frac{dV_{Tn}}{dT} - \frac{\sqrt{\frac{\mu_p W_p}{\mu_n W_n}} d\left|V_{Tp}\right|}{dT} \right)$$

If the temperature is changed, then the effective mobility, channel length, and threshold voltage of the PMOS (V_{Tp}) and NMOS (V_{Tn}) devices will be affected. Therefore, the inverter threshold will also be changed. So the results show that the large ratio of Wp/Wn is more sensitive to temperature variation.

iii. Sensitivity to Power Supply Voltage

Since the CMOS inverter has a single-ended input, it is more susceptible to power supply voltage noise than the differential comparator. The partial differential equation for power supply voltage can be expressed by

$$\frac{\partial V_m}{\partial V_{DD}} = \frac{1}{1+\sqrt{\frac{\mu_n W_n}{\mu_p W_p}}}$$

The lengths of PMOS and NMOS devices are assumed to be equal. This equation also shows that the larger ratio of the Wp/Wn the more sensitive Vm is to power supply voltage variation. Generally, a ±5% power supply range is used in a commercial chip. This rejection ratio will be used in the power supply voltage variation simulation.

3-CONCLUSION

In design of the TIQ Comparator circuits are with different Wp and Wn values and simulated in LT-Spice by using PTM Low Power 32nm Metal Gate / High-K / Strained-Si,CMOS technology with 1V power supply. The static power consumption in TIQ comparator is found to be negligible and so the total power consumption is reduced to its minimum level thereby making this CMOS EIS TIQ comparator acceptable for low power consumption and high speed flash ADC.

REFERENCE

[1] Jincheol Yoo, “A TIQ Based CMOS Flash ADC for System on Chip Application”, A Thesis in Computer Sciences and Engineering, .2003

[2] Ali Tangel and Kyusun Choi, “The CMOS Inverter as A Compactor in ADC Design”, Analog Integrated Circuit and Signal Processing, 39 147-155, 2003

[3] S.S. Khot, P.W.Wani, M. S.Sutaone, Shubhang Tripathi “Design Of A 45 M TIQ comparator for High Speed and Low Power 4-Bit Flash ADC” ACEEE Int. J. On Electrical and Power Engineering Vol.02 No. 01 Feb 2011.

[4] Omar Gonzales, Jonathan Yu, Georgekorbes” 6- Bit Analog to Digital Converter” Dept. of Electrical Engineering, Son Jose State University.

[5] R.Jacob Baker,” CMOS Circuit Design, Layout and Simulation” Second Edition Willey IEEE Press 2004.

[6] Meghana Kulkarni, V.Sridhar, G. H. Kulkarni “The Quantized Differential Comparator in Flash Analog to Digital Converter Design” (IJCNC) Vol.2, No.4, July 2010.

[7] Jincheol Yoo “A TIQ Based CMOS Flash A/D Converter For System-On-Chip Application” PhD Thesis The Pennsylvania State University, 2003.

[8]. R. J. Baker, H. W. Li and D.E Boyce, CMOS Circuit Design, Layout And Simulation, New York, IEEE Press, 2008.

[9]. Sudakar S. Chauhan, S. Manabala, S.C. Bose, and R. Chandel, "A New Approach To Design Low Power CMOS Flash A/D Converter", International Journal of VLSI design & Communication Systems (VLSICS), Vol.2, No.2, June 2011, p.100.

[10]. Dhrubajyoti Basu, Sagar Mukherjee, Dipankar Saha, Sayan Chatterjee, C. K. Sarkar, ”An Optimized Analog Layout for a Low Power 3-bit Flash Type ADC modified with the CMOS Inverter based Comparator Designs”, IEEE Conference on Circuits, Power and Computing Technologies, 2013.
[11]. Pradeep Kumar, Amit Kolhe, "Design & Implementation of Low Power 3-bit Flash ADC in 0.18µm CMOS", International Journal of Soft Computing and Engineering (IJSCE), ISSN: 2231-2307, Volume-1, Issue-5, November 2011. [12]. Sagar Mukherjee, Dipankar Saha, Posiba Mostafa, Sayan Chatterjee, C. K. Sarkar, "A 4-bit Asynchronous Binary Search ADC for Low Power, High Speed Applications, International Symposium on Electronic System Design, 2012.
[13] G. Rajshekhar and M S Bhatt,“Design of resolution adaptive TIQ Flash ADC using AMS 0.35□m technology”, Proceedings of international conference on electronic design, Penang, Malaysia.pp 1-6,December 2008.
[14]http://ptm.asu.edu/modelcard/LP/32nm_LP.pm

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