Comparison between Different Techniques of Digitally Controlled Buck Converter

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Abstract
The objective of this Paper is to study current techniques (Counter comparator method, delay line method) of DPWM generation and to develop new techniques using 8051 for low cost implementation for DC-DC buck converter. In this Paper a novel technique is proposed for PWM generation, which requires Timers and Interrupts of 8051.

Index Terms: *Digitally Controlled DPWM, Resolution, Timer, Interrupts.*

1. Introduction
A **buck converter** is basically a current step up and voltage step down converter. Digital applications like CD Players, DVD Players / Recorders, hi-fi system, mobile charger, pagers, PDAs, laptops, home theatre, televisions and video recorders, these devices require different operating voltages and currents as per their specifications and application. For that a voltage regulator is needed to automatically maintain the regulation for specific product. This voltage regulation can be done by the two following methods
1) Linear Regulator
2) Switching Regulator

Linear Regulator
The resistance of the regulator change in accordance with the load resulting in a constant voltage (output). The regulating device is made to acts like a variable resistor, continuously adjusting voltage divider network to regulate output voltage, and continously dissipating the difference between the input voltages and regulated voltages as a waste heat.

Switching Regulator
The switching regulators are increasing in popularity because they offer the advantages of higher power conversion efficiency and increased design flexibility. A switching regulator work by taking small portion of energy, part by part, from input voltage source, and transfering them to the output. This can be done with the help of a switch and a controller which controls the rate at which electrical energy is transferred to the output hence they called "switching regulator". The regulation is done by using simple switches. These switches changes their state ON and OFF at a fixed rate called as switching frequency, to keep the output at desired level. The output of DC-DC buck converter is given as

$$V_{OUT} = V_{IN} \times \frac{T_{ON}}{T_{SW}}$$

T_{ON} = is on time or duty cycle of the PWM signal.

T_{SW} = is period of PWM signal

The output maximum voltage can be equal to V_{IN} if T_{ON} is same as T_{SW} i.e. 100% duty cycle.

The easiest way to descend the voltage of a DC supply is to use a linear regulator (such as a 7805), but linear regulators wasted energy as they operate by dissipating excess power as mostly in heat. DC-DC Buck converters, on the other hand, can be remarkably more efficient making them useful for different tasks such as converting the main supply voltage in a computer (12 V in a desktop, 12-24 V in a laptop)

2. Digitally controlled DC to DC Buck converter
Digital controllers for DC-DC converters have been verified as having many advantages as compared to the analog controllers. A digital pulse-width modulator (DPWM) of high resolution is used to achieve precise output voltage regulation and eliminate errors to the quantization effects of the ADC and the DPWM.

A/D converter
The ADC converts analog signal in to digital data. These days many advanced microcontroller like PIC, Arduino comes with inbuilt ADC, but the basic microcontroller like 8051 does not have inbuilt ADC.

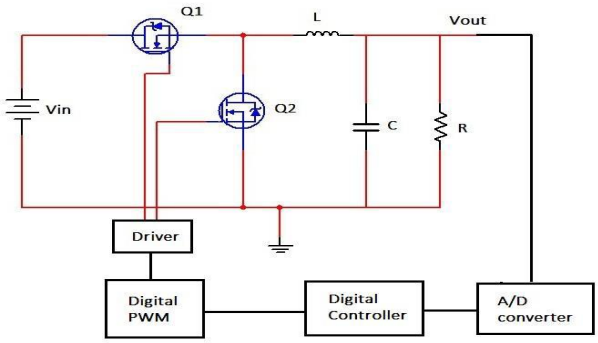

Fig.1 Block diagram of digitally controlled buck converter

Resolution

The resolution of the ADC is defined as number of discrete levels it can produce for the given analog values. The number of discrete values present, or "levels", is a power of two, since they are saved in binary form. ADC's Voltage resolution is equivalent to the reference voltages divided by the number of discrete levels:

$$V = \frac{V_{range}}{2^M - 1}$$

where V_{range} is the full scale voltage range and ADC's resolution is M in bits

$$V_{range} = V_{refHi} - V_{refLo}$$

Where V_{refHi} and V_{refLo} are the upper and lower extremes voltages, respectively.

Pulse Width Modulation

Pulse-width modulation (PWM) is a general technique for controlling over to electrical devices, made practical by up-to-date electronic power switches.

Duty cycle describes the part of 'on' time to the time period; a low duty cycle corresponds to low power, because the supply is off for maximum time. Duty cycle is expressed in percentage, 100% being fully on.

The average value is given by

$$y_{(avg)} = \frac{1}{T}\int_0^T f(t)\,dt$$

If we consider a pulse waveform with a minimun value y_{min}, a maximum value y_{max} and a duty cycle D.

$$y_{(avg)} = \frac{1}{T}\left(\int_0^{D.T} f(t)\,dt + \int_{D.T}^{T} f(t)\,dt\right)$$

$$y_{(avg)} = D \times y_{max} + (1-D)y_{min}$$

If $y_{min} = 0$ Then

$$y_{(avg)} = D \times y_{max}$$

hence average value of the applied signal is directly depend on the duty cycle D.

3. Counter- comparator based technique:

The first method for implementing a DPWM is based on the digital direct emulation of the ramp waveform by using a fast-clocked counter, which is loaded by the input digital codes at the starting of the cycle. This DPWM based on counter follows the general block diagram of Fig.2 An excellent linearity is obtained in the digital to time domain transformation by using of a clock to divide the period of time TSW = 1/ FSW & for an n-bit DPWM. For a high switching frequency FSW and a high DPWM resolution, the requirement of the very high frequency clock is the main demerit of this approach.

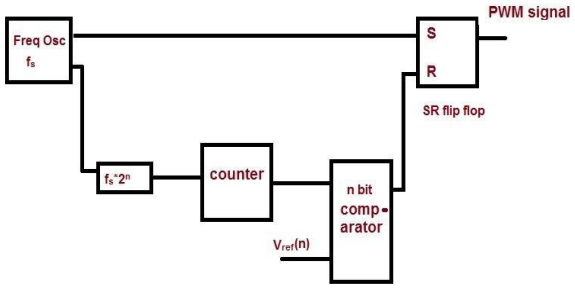

Fig. 2 Block diagram of counter comparator method

The input output relation can be explained as follows with an example. Consider a 3 bit operation, which means all the digital signals are represented and arithmetic operations for them are done using 3 bits and if any arithmetic operation results need more than 3 bits, they are either discarded or stored in other variable. Hence, higher number bit representation gives better resolution consequently less quantization error.

The figures show the output PWM waveform for different reference value. The operation of PWM generation using this counter comparator method. The output of SR flip-flop is set high at the starting of each cycle of switching frequency. The comparator continuously compares the output from the counter with the 3 bit reference value of the voltage. Whenever, the counter values goes above the reference value the comparator makes his carry signal high at the output. This signal triggers the SR flip-flop to reset its output. In fig.3 , the output results are drawn shows the variation in the width of pulse with respect to the error generated by the 3 bit comparator. As it can be seen from the

waveforms generated by the counter, the counter needs to clock at frequency FSW*2n, n is 3 here. That is equal to 8 times the switching frequency FSW. Hence, if we increase the number of bits for high resolution the switching frequency requirement for counter increases exponentially, so this method is not desirable to achieve high resolution.

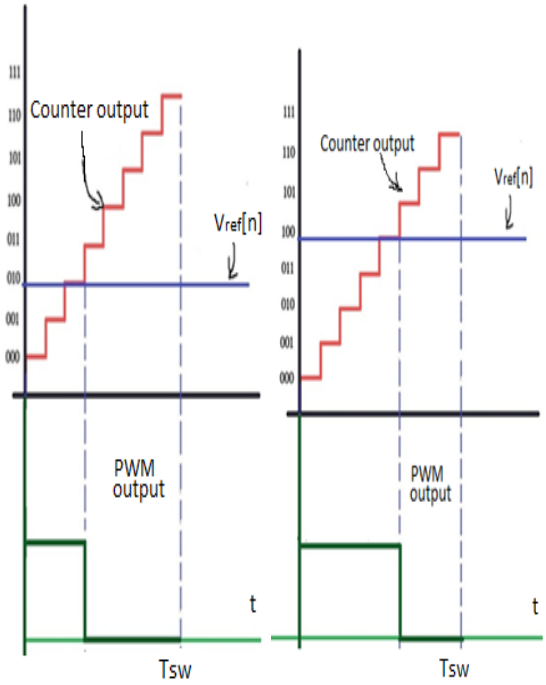

Fig.3 PWM generation using Counter Comparator Method

4. Delay Line based Technique

The second approach is called as Delay line method, it avoids the high-frequency clock problem of the DPWM based on counter, as depicted in Fig 4. This circuit takes benefit of the linear propagation for given pulse from a reference clock clk through the delay cells joined in cascade, to select a given pulses width which quantized as a function of the selected number of cells. This selection can be obtained from the input code by using of a 2n to 1 mux which driven by the digital input code d. The mux selects the signal that resets the PWM output signal, thus executing the task of selecting one of the time slots made by the delay-line time quantizer. The delay line operates in the sense that the switching frequency FSW is imposed by an external oscillator, while the total delay of the line should be considered in order for the maximum delay to match the switching period. As the semiconductor material properties (and therefore the delay of cell td) changes with progression and temperature, this condition cannot be fulfilled at all process or temperature corners. Consequently, the executed duty cycle D_{exe} is not always the similar as the duty cycle command D_{comd} presented by the input digital signal.

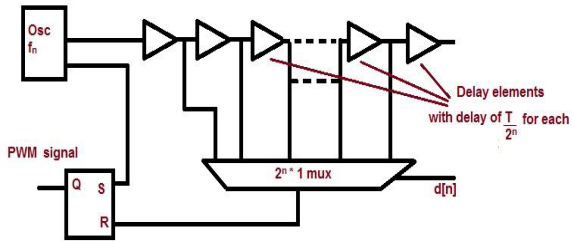

Fig.4 Delay-line based digital pulse width modulator (DPWM) architecture

This method uses N number of delay elements where N is equal to 2n and n is the number of bits, a 2n*1 mux and a flip- flop. The output of each delay element is get delayed by T/2n, where T is total period of switching cycle. At starting each switching cycle, the output of SR flip-flop is set to high, depending on the error d[n] the mux taps one of the delay elements and reset the output of flip-flop. If the error value is high the mux select the more delayed element and the output will be reset lately. In this method the high frequency requirement is circumvented but this method need more number of delay element for higher resolution.

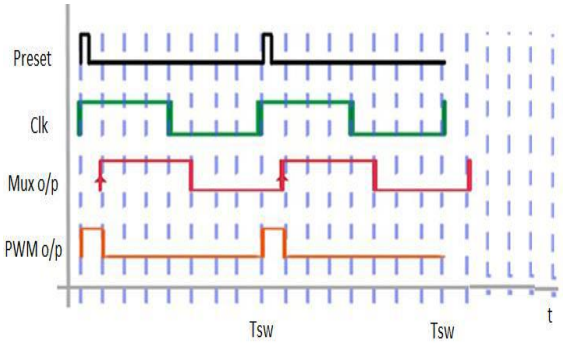

Fig.5 PWM generation using Delay Line Method

This method has disadvantages like the requirement of more hardware as the resolution to increases and hence more delay time is introduced in the control loop which results in slow transient response and reduced bandwidth.

5. Using 8051 Microcontroller

The proposed method for PWM generation is fully based on programming the microcontroller.

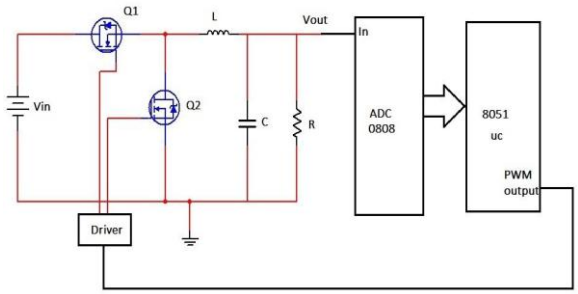

Fig.6 Block diagram for buck converter using microcontroller method

The algorithm of this program is explained by two approaches:
1) Sequential approach
2) Time multiplexed approach

Sequential approach
In this approach microcontroller core processor monitors the timing generation for "ON" and "OFF" status. The program flow is sequential and processor of 8051 is engaged in the time slot generation for PWM signal. The input to this program is the digitized error signal generated from the plant. Digital version of the error signal is generated from the A to D converter used prior to this system. Ton, Toff timing values are calculated depending on the error. These timing values are fed to timer of the 8051 controller and the processor of the 8051 monitors these values and make the PWM output from the 8051 high and low representing "ON" and "OFF" status of the pin.

Time multiplexed approach
For this approach the concept of interrupts is exploited. by some event an interrupt is triggered, externally to the current operating program. We can say that interrupt event happens asynchronously to the presently operating program as it is not essential to know in spread when the interrupt event is going to happen. There are total six interrupt sources for the 8051.

Interrupt	Flag	Vector address
System RESET	RST	0000h
External interrupt 0	**IE0**	**0003h**
Timer/counter 0	TF0	000Bh
External interrupt 1	**IE1**	**0013h**
Timer/counter 1	TF1	001Bh
Serial port	RI or TI	0023h

Fig.7 Interrupt with flag and vector address

The time multiplexed approach uses timer and external interrupt of 8051. These interrupts will produce an interfere to current process and make the processor to respond it. To respond the interrupt the microcontroller executes an interrupt handler program which is also called as Interrupt Service Routine (ISR). At this location the respective instructions are saved which will be executed when the processor transfers the program control here.
Here at the ISR of timer 0, instructions for toggling the status of PWM output depending on T_{ON} and T_{off} are saved and at the ISR of external interrupts a small program is written to update the T_{ON} and T_{off}.

6. Conclusion
Counter comparator method of DPWM provides good linearity in digital to time domain conversion and fail to provide high resolution. The counter also requires high very clock frequency i.e. FSW*2n, where FSW is switching frequency and *n* number bits.
The drawbacks of counter comparator methods are circumvented in delay line method. But this delay line method requires more hardware and the number of delay elements increase with increase in the number of bits. One more disadvantage of this method is, the temperature effect on the semiconductor devices.
The proposed approach eliminates drawbacks of counter comparator method and delay line method. It provides good linearity between the digital to time domain conversion. The switching frequency can be increased by increasing the clock frequency of the microcontroller. The proposed method produces quantization error due to the ADC resolution and the slots of timer used in microcontroller. These errors can be reduced by increasing the resolution of ADC and clock frequency of the microcontroller.

7. Future work
The proposed method does not incorporate any controller like PI, PID, though the problem of saturation is taken care by the program. Hence the immediate future work would be to use a suitable controller for efficient controlling and make the system more stable.
As the proposed method uses basic 8051 architecture, there is limitation on the speed of operation consequently there is limitation on the high frequency PWM generation. This can be circumvented by using high speed microcontroller or even using the FPGAs for PWM generation.

References

[1] Asif Syed, Ershhad Ahmed and Dragan MaksimooviC, Eduard Alarcon "Digital Pulse Width Modulator Architecture", 351 h Annual Conference IEEE Power Electronics Specialirls Aachhen, Germany, 2004.

[2] Santa Concepcion Hueerta, Angel de Castro, Oscar Garcia, and Jose A. Cobos "FPGA-Based Digital Pulsewidth Modulator With Time Resolution Under 2 nsec", IEEE Transaction on Power Electronics Vol. 23 No.6, pp. 3135-3142, November 2008

[3] Soon H. Kwon Ieck Choy and K. H. Kim H. S. Mok, "A New Direct Digital PWM Technique for Microprocessor-Base PWM Inverter", Power Electronics Specialists Conference, 1996. PESC 96 Vol. 2 pp.: 1300 – 1304.

[4] Brigite Hauke "Basic Calculation of a DC-DC Buck Converter's Power Stage" an Application Report December 2011–Revised August 2012.