Dynamic Threshold MOS transistor for Low Voltage Analog Circuits

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ABSTRACT

Due to larger driving ability with low leakage current, the Dynamic Threshold MOSFET(DTMOS) is attractive for low power applications. Additionally as transistors always work in the saturation region for analog and RF applications, the analog characteristics of DTMOS in saturation region are also attractive. The performance of analog circuits strongly depends on how the characteristics of the transistors are exploited and mastered. In DTMOS, body has important influence in the device behavior. It is then necessary to model it properly. For this purpose a new equivalent circuit has been introduced to present the description about contribution of body conductance in Bulk-DTMOS, from the perspective of the circuit designer. We have presented a systematic study and development of new small signal Bulk DTMOS model to assist circuit designers carrying out hand calculations with easily manipulated expressions for low voltage (<0.6V) analog circuits.

Keywords *- Analog circuits, Bulk-Dynamic threshold MOS transistor, Body bias, Body effect, Low voltage, Small signal model*

I. INTRODUCTION

There is an increasing interest in the suitability of Bulk-DTMOS for analog applications. Over many years debate has continued over whether SOI or Bulk would prove to be the most suitable for low voltage analog circuits. Scalability of SOI technology for analog performance provides no significant advantage over bulk technology. SOI parameters that scale poorly are history effect and junction capacitance. The impact of junction capacitance diminishes with scaling. SOI shows a reduced role for junction capacitance and an increased history effect for scaled devices, so that SOI has significantly diminished performance gain relative to bulk CMOS for 50nm devices. Self heating effects are much more apparent in SOI than in Bulk due to poor thermal conductivity of the underlying buried oxide and device temperature can rise dynamically many tens of degrees above ambient during normal operation. Thermal behavior is not generally significant for digital circuits but analog circuits, however can be significantly affected. The effects of the floating body in SOI are far more serious for analog design. The well known kink effect leads to large sensitivity and frequency dependent variations within normal operating regimes. For the frequencies in the range of GHz where kink effect is totally suppressed, analog performance of SOI devices is inferior to that of the bulk devices due to capacitive drain to body coupling. As gate oxide is reduced to less than 2nm, gate leakage and the reduced supply voltage can seriously affect many analog circuits [1-4].

MOSFET has conflicting device performance requirements for digital and analog circuits. International technology roadmap for semiconductors has two different scaling guidelines for analog and digital circuits with analog device design lagging behind the digital by 3-4 technology generations. For analog circuits intrinsic gain (g_mR_{out}), cutoff frequency (f_t), g_m/I_{ds} ration, linearity, noise and device mismatch constitute the performance metric. Optimizing the MOSFET for one of them often leads to degradation in the others[5-6].

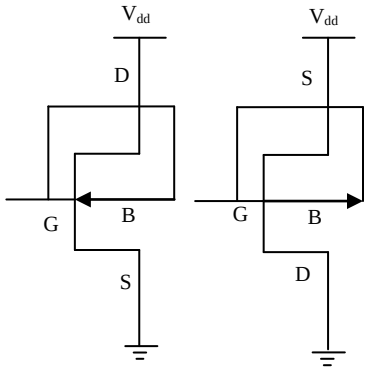

Fig.1: NMOS & PMOS transistors based on DTMOS circuit Topology

When body and gate of a MOSFET are tied together, this configuration is known as DTMOS as seen in Fig.1. The threshold voltage of a DTMOS transistor is given as

$$V_{th} = V_{tho} - \gamma\sqrt{2\emptyset_F} + \sqrt{2\emptyset_F - V_{BS}} - \eta V_{DS} \quad (1)$$

Where, V_{th} is threshold voltage when V_{SB} is not zero, V_{tho} is the zero body bias threshold voltage and mainly depends on the manufacturing process. γ is the body effect coefficient (typically equals to 0.4 $V^{0.5}$) and it depends on the gate oxide capacitance, silicon permittivity, doping level and other parameters. Φ_F is the surface potential at threshold (typically $|-2\varphi_F|$ equals 0.6 V). V_{SB} is the source-to-body voltage. The term ηV_{DS} represent the effect of Drain-Induced Barrier Lowering (DIBL) in which η is the DIBL coefficient and it is in the range of 0.02–0.1. From (1) it can be seen that the threshold voltage depends on V_{SB} which in turn affects the depletion region charge density or body charges. Forward bias across the junction reduces the junction width and hence depletion region charge density which in turn reduces V_{th}. Reverse bias increases the depletion region width and hence increases body charges due to which V_{th} also increases. As DTMOS based circuits make use of forward bias, therefore when input is high, the transistor will be on resulting in reduction of V_{th} and higher driving capability. When the transistor is turned off, V_{th} becomes high, resulting in low leakage current. Thus the threshold voltage is changed dynamically according to the input at the gate i.e. operating state of the circuit. Thus DTMOS enables the circuit to operate under the low voltage supply hence suitable for low voltage operation due to its dynamic threshold voltage, larger transconductance, and lower noise [7-12].

Transistors always work in the saturation region for analog and RF applications, therefore analog and RF characteristics of DTMOS in saturation region are also attractive. The performance of analog circuits strongly depends on how the characteristics of the transistors are exploited and mastered.

DTMOS technique can be applied to both NMOS and PMOS in the SOI technology, however the same technique cannot be applied to the NMOS transistors in the conventional Bulk-CMOS technology because all NMOS transistors share the same substrate, it can only be applied to the PMOS transistors since every transistor is isolated in its own n-well. To extend the application of the DTMOS to the NMOS in Bulk-CMOS technology triple well has to be used [13-14]. Many bulk-DTMOS based applications have been reported in literature [15-21]. But a small signal model is required as a preliminary for hand calculations for analog circuits.

In this paper a small signal model is proposed to analyze analog characteristics of Bulk-DTMOS. The useful effect of the DTMOS is related to the body conductance (g_{mb}) of the transistor. In this work, we would like to present a new description i.e. contribution of body conductance in Bulk-DTMOS model. In section II, physics of Bulk-DTMOS is presented and its principle of operation is discussed. In section III, small signal model suitable for hand calculations is proposed. Conclusions are summarized in section IV.

II. BULK DTMOS DEVICE PHYSICS

Any MOSFET has an intrinsic BJT and diodes embedded in its structure as shown in fig. 2.

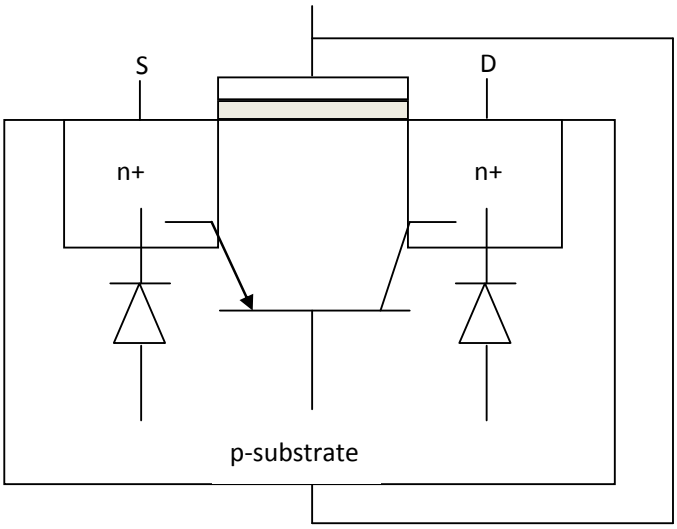

Fig.2: Intrinsic BJT and diodes embedded in NMOSFET structure

The Bulk-DTMOS has inherent parasitic bipolar effect. It is assumed that the MOSFET current flows close to the channel surface and bulk parasitic BJT current flows through the bulk region, therefore the interaction between these two currents can be neglected. We will limit the scope of our study to values of gate/body voltage <0.6V. Under these bias conditions the parasitic BJT is off. Hence only Body-Source junction diode and Body-Drain junction diodes contributes to the body current. We can observe from drain current characteristics of DTMOS [22] in fig.3 that DTMOS current saturates for drain voltages above 0.15V for gate/body input of 0.2V to 0.6V. Thus body-drain diode also remains forward biased and for analog applications DTMOS works in saturation region. Thus the total current of DTMOS for analog applications is mainly due

to two components. First is due to surface MOS operating in saturation region component. Second is due to forward biased Body-Source and forward biased Body-Drain junction diodes.

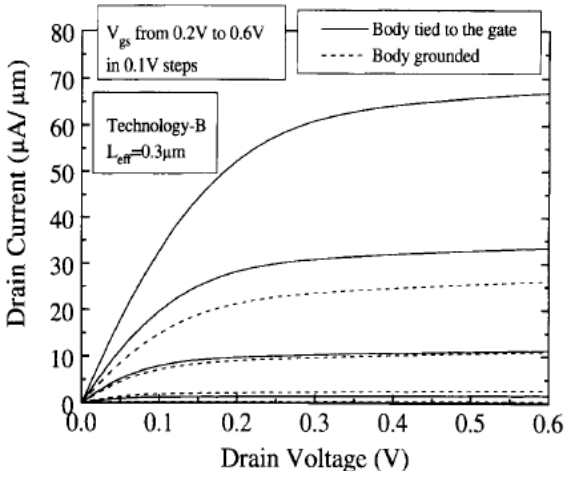

Fig.3: Drain current of an NMOS operated as DTMOS

We assume initially that in the ideal diode there is no recombination of the electron and hole injected currents in the depletion region [23]. The ideal diode current I_{Diode} flowing in forward biased junction can be written as

$$I_{Diode} = qA\left(\frac{D_p}{L_p}p_n + \frac{D_n}{L_n}n_p\right)\left(e^{\frac{qV}{KT}} - 1\right) \quad (2)$$

$$I_{Diode} = I_o\left(e^{\frac{qV}{KT}} - 1\right) \quad (3)$$

where the prefactor I_o is given by

$$I_o = qA\left(\frac{D_p}{L_p}p_n + \frac{D_n}{L_n}n_p\right) \quad (4)$$

Where p_n is hole density on n side, n_p is electron density on p side,V is voltage across the diode, A is diode junction area, D_p is diffusion coefficient of holes, D_n is diffusion coefficient of electrons, L_p is diffusion length of holes, L_n is diffusion length of electrons. However in a real diode, a number of sources may lead to bandgap states that may lead to trapping. The states may arise if the material quality is not very pure, so that there are chemical impurities present. The doping process itself can cause defects such as vacancies, interstitials etc. Let us assume that the density of such deep level states is N_t and that deep level is at the center of the bandgap. The electron-hole recombination rate per unit volume is given by

$$R_t = \frac{np}{\tau(n+p)} \quad (5)$$

where n is electron concentration, p is hole concentration and τ is the recombination time given by

$$\tau = \frac{1}{N_t\, v_{th}\, \sigma} \quad (6)$$

where v_{th} is thermal velocity of the electron(assumed the same for the hole) and σ is the capture cross-section of the trap for the electron or hole. As electrons and holes enter the depletion region, one possible way they can cross the region without overcoming the potential barrier is to recombine with each other. This leads to an additional flow of charged particles. This current, called the generation-recombination current, must be added to the I_{Diode}.

The generation-recombination current $I_{GR}$is

$$I_{GR} = \frac{qAW_d n_i}{2\tau} exp\left(\frac{qV}{2kT}\right) \quad (7)$$

$$I_{GR} = I_{GRo}\, exp\left(\frac{qV}{2kT}\right) \quad (8)$$

where the prefactor I_{GRo} is given by

$$I_{GRo} = \frac{qAW_d n_i}{2\tau} \quad (9)$$

Thus in a real diode total current becomes

$$I_{RDiode} = I_{Diode} + I_{GR} \quad (10)$$

The prefactor I_{GRo} can be much larger than prefactor I_o for real devices. At low biases (< 0.5V) the recombination effects are quite pronounced, while at higher biases (0.5V-0.8V) the diffusion current starts to dominate. At still higher biases the behavior becomes more ohmic due to high injection effects [23].

At low biases (< 0.5V) as the case is for DTMOS

$$I_{RDiode} \cong I_{GR} \quad (11)$$

$$I_{RDiode} \cong \frac{qAW_d n_i}{2\tau} exp\left(\frac{qV}{2kT}\right) \quad (12)$$

$$I_{RDiode} \cong I_{GRo} exp\left(\frac{qV}{2kT}\right) \quad (13)$$

III. SMALL SIGNAL MODEL

We have proposed an equivalent small-signal circuit for DTMOS including the body contact network based on the well known four terminal model of the MOSFET [24] shown in Fig.4. It has been proposed that both the body-source and body-drain junctions remain forward biased in DTMOS device. We have tried to accurately describe the forward biasing of body through $g_{mb}(V_{bs}+V_{bd})$.

Total input gate capacitance C_{gg} is

$$C_{gg} = C_{gs} + C_{gd} \quad (14)$$

As the body and gate are connected together through R_{body} the total gate/body to source transconductance is equal to g_{gg}.

Total gate transconductance is

$$g_{gg} = g_m + g_{mb} \quad (15)$$

Bulk substrate network is crucial for describing output impedance behavior accurately. Good accuracy is achieved with just a single bulk resistor. Additional improvement is achieved by increasing the number of resistors to three. Based on the equivalent circuit, it is possible to develop approximated expressions for total current in Bulk-DTMOS. The approximate equation of the drain current, considering that at low frequencies, the effect of gate, drain and source resistance are negligible compared to R_{body}

$$I_{DTMOS} = I_{MOS} + I_{Diode(bs)} + I_{Diode(bd)} \quad (16)$$

$$I_{DTMOS} = \frac{\mu_n C_{ox} W}{2L}(V_{gs} - V_{th})^2 + \frac{qAW_d n_i}{2\tau} exp\left(\frac{qV_{bs}}{2kT}\right) + \frac{qAW_d n_i}{2\tau} exp\left(\frac{qV_{bd}}{2kT}\right) \quad (17)$$

The impact of the gate potential on the drain current is given by transconductance. For DTMOS body potential is same as gate potential i.e. $V_b=V_g$

$$g_m = \frac{\partial I_{DTMOS}}{\partial V_{gs}} \quad (18)$$

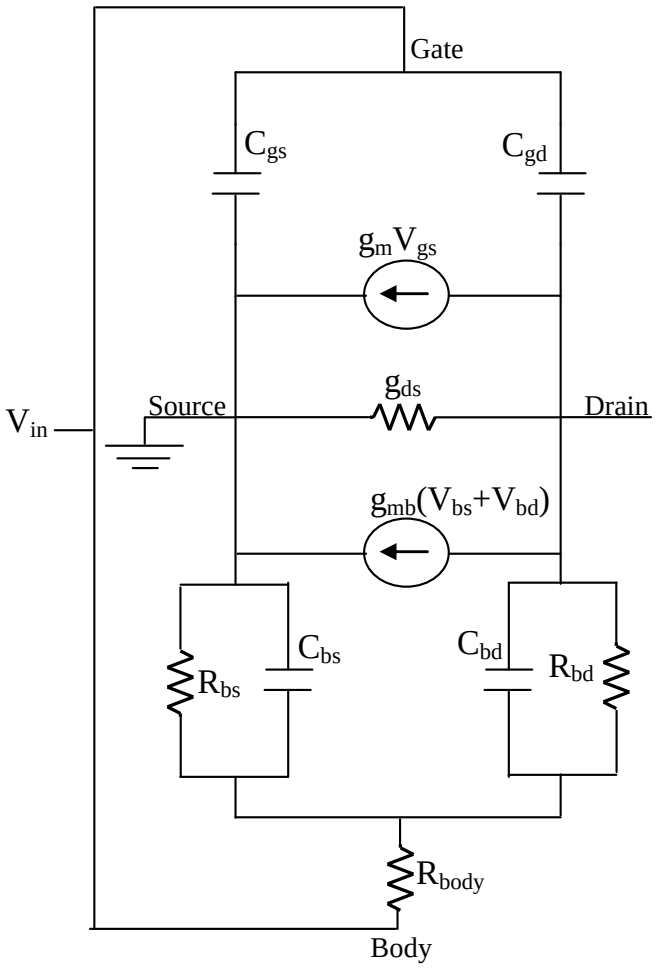

Fig.4: Proposed small signal equivalent circuit of Bulk-DTMOS

The approximate equation of transconductance derived from above equation is

$$g_m = \frac{\mu_n C_{ox} W}{L}(V_{gs} - V_{th}) + \left(\frac{q}{2kT}\right)\frac{qAW_d n_i}{2\tau} exp\left(\frac{qV_{gs}}{2kT}\right) \quad (19)$$

$$g_m = \frac{\mu_n C_{ox} W}{L}(V_{gs} - V_{th}) + \left(\frac{q^2 AW_d n_i}{4\tau kT}\right) exp\left(\frac{qV_{gs}}{2kT}\right) \quad (20)$$

The impact of the body potential on the drain current is given by body transconductance

$$g_{mb} = \frac{\partial I_{DTMOS}}{\partial V_{bs}} + \frac{\partial I_{DTMOS}}{\partial V_{bd}} \quad (21)$$

Before the gate voltage is lower than the threshold voltage, the MOS part is in cutoff region. As the gate voltage is higher than the threshold voltage, the MOS enters into the saturation region and both diodes starts to work so transconductance increases more rapidly as illustrated by two terms of (21)

The resistive network representing substrate is a π shaped model and can be transformed into a T shape model. Both gate and body transconductance directly contribute to current gain of Bulk DTMOS.

IV. CONCLUSION

Based on measured data available, we have developed a new small-signal equivalent circuit model that has an additional current source $g_{mb}V_{bd}$ to express body effect correctly. Using this model, we studied the body contribution of the DTMOS in low voltage analog circuits(<0.6V).The small signal model for DTMOS device proposed in this paper is for long channel. DTMOS can be considered to be one of the most promising devices for low power analog/RF circuits.

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