High Speed & Power Efficient Inverter using 90nm MTCMOS Technique

Buddhi Prakash Sharma[1]
ME Scholar, Electronics & Communication
NITTTR, Chandigarh, India

Rajesh Mehra[2]
Associate Professor, Electronics & Communication
NITTTR, Chandigarh /Ministry of HRD Govt. of INDIA

ABSTRACT
A high speed and low power CMOS inverter is designed & simulated in this paper. The critical path consists of PMOS and NMOS. The designed inverter cell offers high speed and low power consumption than the CMOS inverter. A Multi Threshold Complementary Metal Oxide Semiconductor (MTCMOS) technique is used to reduce the leakage current as well as leakage power to achieve better results. MTCMOS is very effective circuit level technique that improves the performance in terms of power by utilizing low and high threshold voltage transistors. Leakage current of CMOS inverter is reduced by 30.77% in case of Low Leakage and 29.48% in case of High speed operation using MTCMOS technique. Leakage power of the MTCMOS inverter therefore reduced as leakage current reduced. The Schematic of developed inverter has been designed using DSCH and its layout has been created using 90nm technology in microwind 3.1 tool.

Index Terms- CMOS, MTCMOS, Inverter, Leakage Current, Threshold

I. INTRODUCTION
Great attention has been focused on low-power microelectronics due to the rapid development of laptops, portable systems, and cellular networks. Low power consumption has become a major consideration in circuit design [1]. The most conventional CMOS (complementary metal oxide field effect transistor) inverter design is combination of PMOS (P-channel MOSFET) and a NMOS (N-channel MOSFET).CMOS is also known as COS-MOS (Complementary and symmetrical pairs of P-channel and N-channel MOSFET for logic function. The size of the transistors is reduced with technology scaling, thereby increasing the integration density and the operating speed of the circuits [2]. A low power design is essential to achieve long battery life in battery-operated devices. With the current scenario of semiconductor devices scaling into nanometer region, design challenges are becoming more important where in the past dynamic power has been the major factor in CMOS digital circuit power consumption, recently with the dramatic decrease of supply and threshold voltages, a significant growth in leakage power demands new design methodologies for digital integrated circuits to meet the new power constraints. As one of the major components which affect the leakage current is sub threshold leakage which is caused by the current flowing the transistor although it is turned off. The scaling down the feature size of the transistor exponentially increases the impact of sub-threshold leakage. Many techniques have been proposed to control as well as minimize leakage power in nanometer technology. Overweening power dissipation in digital integrated circuits, not only affects their use in portable devices but also causes overheating, degrades performance, reduces chip life and functionality. Reducing power consumption is most important and necessary, both for increasing levels of integration and to improve feasibility and cost as well as reliability. In this paper we use MTCMOS (multi-threshold CMOS) technique for designing of high speed and power efficient CMOS inverter in 90 nanometer technology. MTCMOS technique has been emerged as a promising alternative to build logic circuits operating at a high speed with relatively low power dissipation as compared to traditional CMOS [3]. MTCMOS is an effective circuit level technique that increases the performance and provides low design methodologies by using both high and low threshold voltage transistors. This paper is organized as follows section2 gives a brief description of designing inverter using CMOS technique and section3 presents designed MTCMOS technique for inverter. Section4 presents the details of leakage current and introduces leakage power of the CMOS inverter combinational circuit as well as the simulation results of the CMOS inverter in terms of leakage current and leakage power& section5 concludes this paper.

II. CMOS BASED DESIGN SIMULATION
In case of planar CMOS inverters, symmetry in rise and fall time are achieved by choosing the W (width) of PMOS transistor to be twice than that of NMOS device with the same length *L*, to compensates for the low value of the hole mobility. The inverters maintain their good transfer characteristics and noise margins for a wide range of V_{DD} values, down to 0.2V. Short circuit current at 0.2V V_{DD} is approx 0.6 pA (pico ampere) indicating excellent potential of these devices for low voltage and ultra low power applications [4]. Inverter is the most fundamental part in any logic and most of the other basic

operators such as NOR and NAND are realized according to its structure. Hence designing an efficient inverter cell leads to enhancement of overall system performance. In addition to the inversion operation, the inverter is also a great driver and its driving capability is very important [5]. In digital circuit theory, combinational logic is a type of digital logic which is implemented by Boolean circuit, where the output is a function of the present input only. This is in contrast to sequential logic, in which the output depends on the present input as well as on the history of the input (past output). In other words, sequential logic has memory while combinational logic does not.

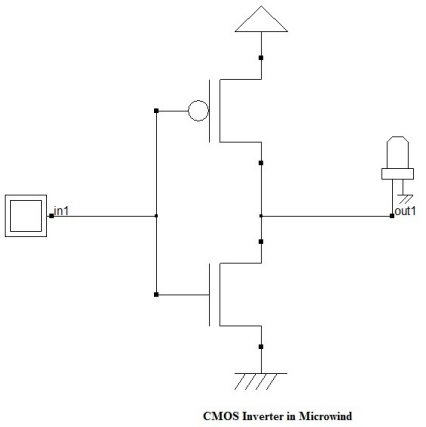


Figure 1: CMOS Inverter cell

Inverting operation can be understood by the following truth table:

Table 1: Inverter truth table

INPUT	OUTPUT	LED
0 "when switch is off"	1	GLOW
1 "when switch is on"	0	NOT GLOW

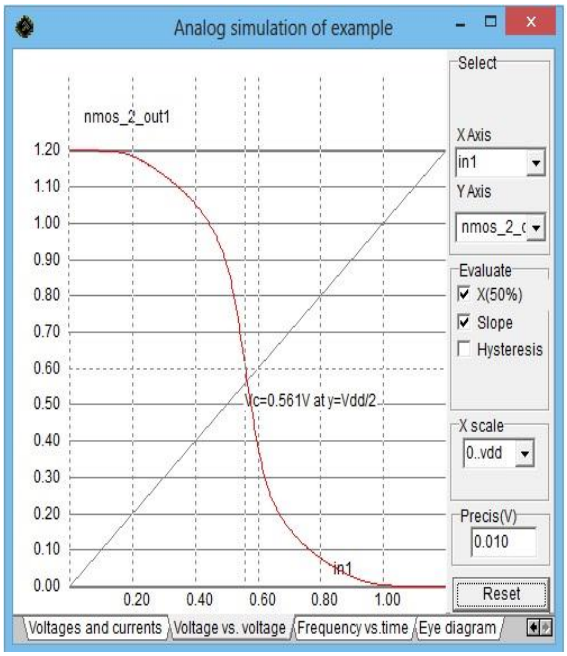


Figure 2: CMOS Inverter Cell Output

In fig. 1 CMOS inverter cell having a PMOS and a NMOS both are complementary to each other. When logic "1" input is given to switch NMOS (pull down network) is active and output (LED) is connected to ground. In other case, when switch is in logic "0" state PMOS (pull up network) is active and at this time output is connected to V_{DD}. Figure 2 shows CMOS inverter layout design which is implemented by basic CMOS inverter cell in microwind.

Combinational logic is used in computer circuits to solve boolean function on input signals and on stored data. Figure 3 shows layout designs of inverter cell.Practical computer circuits normally contain a mixture of combinational and sequential logic to implement any design. For example, the part of an ALU (arithmetic logic unit), that does mathematical calculations is constructed using combinational logic. Other circuits used in computers, such as half subtractors, full subtractors, multiplexer, demultiplexer, half adders, full adders, encoders and decoders are also made by using combinational logic. So inverter is a basic cell to design any kind of digital circuit. Figure 1 shows basic CMOS inverter cell implemented in microwind tool.

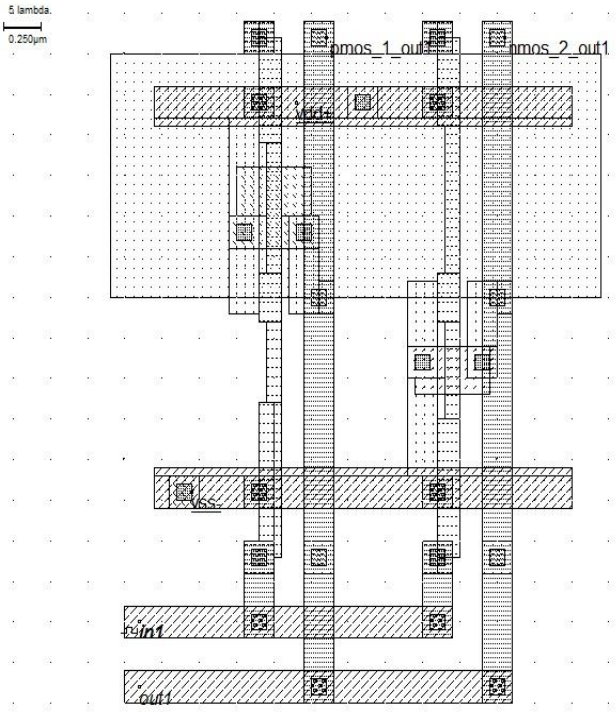


Figure 3: CMOS Inverter Cell Layout

III. MTCMOS BASED DESIGN SIMULATION

The scaling of CMOS technology in nanometer technology effectively reduces supply voltage and threshold voltage. Lowering of threshold voltages leads to an exponential increase in the sub-threshold leakage current [6]. Overweening power dissipation in digital integrated circuits, not only affects their use in portable devices but also causes overheating, degrades

performance, reduces chip life and functionality. In the modern high performance integrated circuits, more than 40% of the active mode power is dissipated due to the leakage current. As number of the transistor increases on a chip, leakage current effects the total power consumption of the integrated circuit. The new MTCMOS technology is proposed to satisfy both requirement of reducing standby current and lowering the threshold voltage of transistor, both which is necessary to obtain low power and high speed performance at the supply voltage. This technology has two main features. One is that PMOS & NMOS transistors with two different threshold voltages are employed in a single chip [7]. The second one is two operational mode active and sleep for efficient power management. In MTCMOS

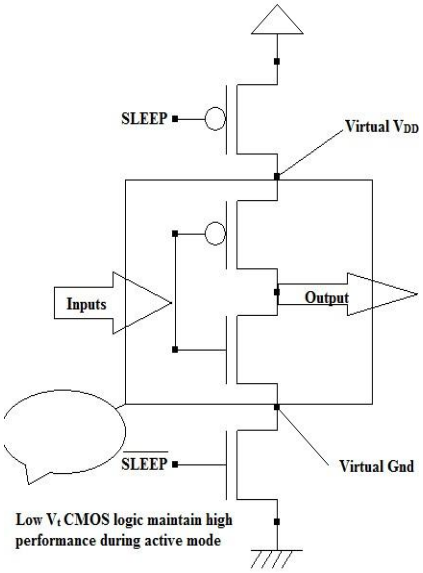


Figure: 4 General MTCMOS Circuit Architecture

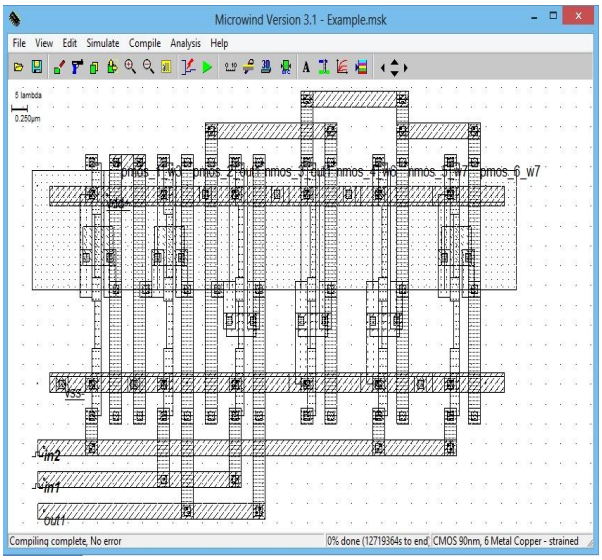
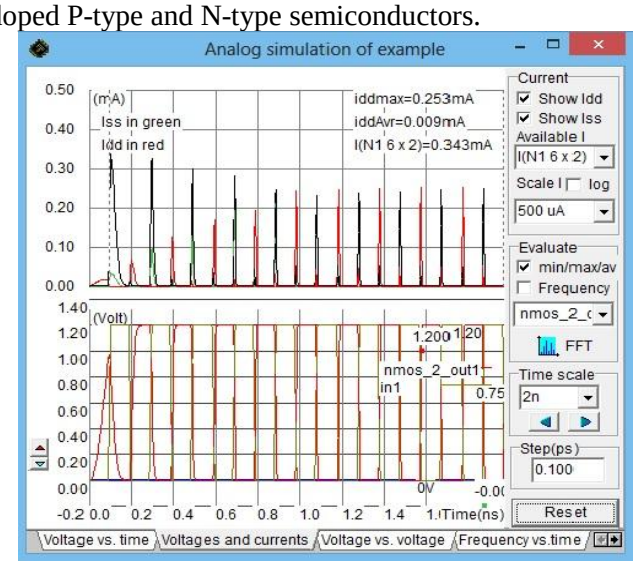


Figure: 5 MTCMOS inverter Layout

technique, transistors of low threshold voltage becomes disconnected from power supply by using high threshold sleep transistor on the top and bottom of the logic circuit. Transistor having low threshold voltage (low V_{th}) is used to design logic as shown in figure 3. This is a State-destructive technique which cuts off either pull-up or pull-down or both the networks from supply voltage or ground or both using sleep transistors shown in figure 4. This technique is MTCMOS, which adds high-V_{th} sleep transistors between pull-down networks and gnd, pull-up networks and V_{DD} while for fast switching speeds, low-V_{th} transistors are used in logic circuits [8]. Isolating the logic networks, this technique dramatically reduces leakage power during sleep mode. However, the area and delay are increased due to additional sleep transistors [9]. During the sleep mode, the state will be lost as the pull-down and pull-up networks will have floating values. These values impact the wakeup time as well as energy significantly due to the requirement to recharge transistors which lost state during sleep mode. This results a very low sub-threshold leakage current power to ground when the circuit is in standby mode. Figure 5 represent the layout design of MTCMOS inverter cell. One drawback of this method is that portioning and sizing of sleep transistors is difficult for large circuits.

IV. RESULT ANALYSIS & DISCUSSION

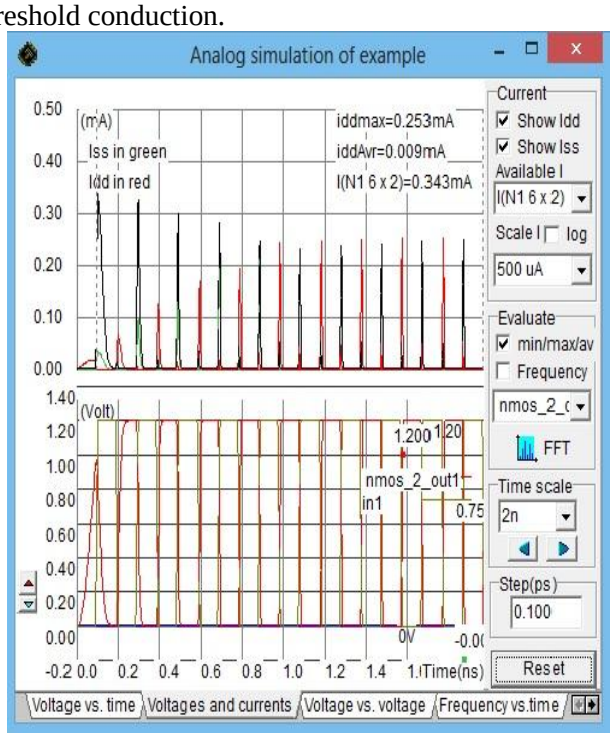
Leakage current and power are an important factor for any CMOS circuit design. The leakage current is directly related to the electric field of the device. By reducing the node voltages decrease the leakage current. In other words we can say when device is in off state, Leakage current or power is a waste charge which is regularly discharging from the device. It reduces the capability of the device results in poor performance of device. Leakage increases exponentially as the thickness of the insulating region decreases. Leakage (tunneling) can also occur across semiconductor junctions between heavily doped P-type and N-type semiconductors.



(a)

Other one is the gate insulator or junctions, carriers can also leak between source and drain terminals of a Metal

Oxide Semi-conductor transistor. This is known as sub threshold conduction.



(b)

Figure: 6 CMOS inverter cell simulation result

The leakage current of a CMOS transistor consists of three main components: gate tunneling current, sub threshold current, and junction tunneling current. Leakage increases power consumption and if it is large can cause complete circuit failure. Analog simulation results are represented in figure 6 (a), (b) in microwind 3.1 tool. Static CMOS gates it is very power efficient. Earlier, the power consumption of CMOS devices was not the major concern in chips designing. Speed and Area are dominant designing parameters. As the CMOS technology moved below sub-micron levels the power consumption per unit area of the chip has risen tremendously. Here we use a CMOS technology to reduce the leakage current/power of inverter at 90 nanometer technology. The leakage power is one of the major sources of power consumption in high performance cell. The leakage power dissipation is roughly proportional to the area of the circuit. The leakage power dissipation is expected to become a significant fraction of the overall chip power dissipation in nanometer CMOS design process [10]. In CMOS technology standby power consists of leakage-power which increases with each silicon-technology generation [11]. Thus, for low power devices like sensor nodes, standby leakage power reduction is crucial for device operation within the scavenging power limit [12].

The leakage current in MOSFETs depends on various process parameters, the transistor size W/L (Aspect ratio), N-factor, temperature etc. Leakage current doubles for every 8^0 to 10^0 K rise in temperature.

In CMOS circuit design, the total power dissipation includes dynamic and static components during the active mode of operation but in case of the standby mode, the power dissipation is due to the standby leakage current. The dynamic switching power $P_{DYNAMIC}$ and leakage power ($P_{LEAKAGE}$) are expressed as:

$$P_{DYNAMIC} = \beta f C V_{DD}^2 \qquad (1)$$

$$P_{LEAKAGE} = I_{LEAKAGE}.V_{DD} \qquad (2)$$

Where β is the switching activity; f is the operation frequency, C is the load capacitance, V_{DD} is the supply voltage and $I_{LEAKAGE}$ is the cumulative leakage current due to all the components of the leakage current.

Inverter is a combinational circuit that performs the inverting operation (complement) of the given input. In this paper we simulate CMOS inverter in 90 nanometer technology by microwind 3.1tool. Here we proposed MTCMOS technique that effectively reduces leakage current ($I_{LEAKAGE}$) and leakage power of CMOS inverter cell as compared to CMOS technique. Figure 6 and figure 7 shows the simulated results of inverter cell using CMOS technique and MTCMOS technique respectively. CMOS inverter cell simulated results are shown in table2 at different temperature for low leakage and high speed analysis. Likewise table 3 provides the information of inverter cell using MTCMOS technique. These tables 2, 3 clearly show that as temperature increases $I_{LEAKAGE}$ also increases. Leakage current also increases as value of N-Factor increases.

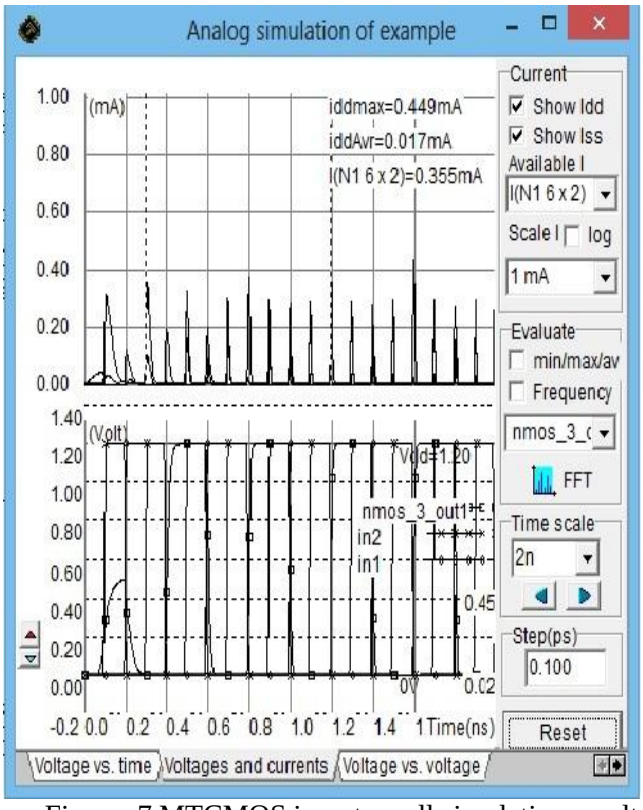


Figure: 7 MTCMOS inverter cell simulation result

Table: 2 Simulation results of CMOS inverter cell

Low Leakage (W=1µm,L=0.1µm)				High Speed (W=1µm,L=0.1µm)		
Temperature(^{O})	I_{DRIVE} (mA)	$I_{LEAKAGE}$ (nA)	$I_{LEAKAGE}$	I_{DRIVE} (mA)	$I_{LEAKAGE}$ (nA)	$I_{LEAKAGE}$ (nA)
-13.00	.366	0	0	0.425	2	4
7.00	.339	2	3	0.397	24	32
27.00	.316	13	17	0.372	173	203
47.00	.294	59	73	0.350	893	969
N Factor→		0.9	1.0	N Factor →	0.9	1.0

Table: 3 Simulation results of MTCMOS inverter cell

Low Leakage (W=1µm,L=0.1µm)				High Speed (W=1µm,L=0.1µm)		
Temperature(^{O})	I_{DRIVE} (mA)	$I_{LEAKAGE}$ (nA)	$I_{LEAKAGE}$	I_{DRIVE} (mA)	$I_{LEAKAGE}$ (nA)	$I_{LEAKAGE}$ (nA)
-13.00	.433	0	0	0.495	2	2
7.00	.399	1	2	0.459	17	22
27.00	.368	9	12	0.426	122	146
47.00	.341	41	52	0.397	653	718
N Factor→		0.9	1.0	N Factor →	0.9	1.0

V. CONCLUSION

In this paper we proposed a MTCMOS technique that greatly reduces the power dissipation of the inverter cell. Finally it is concluded that MTCMOS technique is better as compared to normal CMOS technique. MTCMOS is an effective circuit level technique that enhances the performance and provides low design methodologies by using both low and high threshold voltage transistors. From the simulation result it is cleared that after applying this technique we have reduced leakage current in both low leakage and high speed operation. So by using MTCMOS technique we designed a high speed and power efficient inverter cell.

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