AREA EFFICIENT 5-INPUT DECIMAL ADDER

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ABSTRACT- With the increasing complexity in computation application we need better decimal adder which takes lesser time and less power consumption. So in this paper we have proposed an area efficient 5-input decimal adder using sum vectors and correction bits. With the help of carry look ahead adder, generator circuit our designed decimal adders could perform efficient addition with five input operands. In our implementation after synthesize through Xilinx verilog module we get delay of 12.352 ns which is less with increased number of inputs.

KEYWORDS- ***VLSI design, BCD adder, CLA, CSA, DG, DP.***

INTRODUCTION-

In earlier time binary arithmetic is commonly used for computation in computers and processors. But binary arithmetic expressions are not sufficient or we can say binary arithmetic unable to fulfil the requirement of fractional terms. Like in $(.33)_{10}$ $=0.0101...._2$ it requires infinite bits for representation, thus causing inexact results so we use approximation but this will not give us an efficient output. Fractional terms are very oftenly used in commercial fields and efficient output is must requirement so we use Binary Coded Decimal (BCD) numbers to represent decimal numbers.

In BCD each decimal digit is represented in 4-bit BCD numbers from 0 to 9.For example $(0.8)_{10}$= $(0.1000)_2$ we get finite and exact representation.

So we work on 5-input decimal adder . Our proposed work is designed to give hardware support for decimal arithmetic but when addition of two BCD numbers is greater than 9 we use correction logic which add (0110) in each nibble.

So 5-input decimal adder is proposed to reduce chip area, less power consumption with optimize propagation delay than previously proposed adder and also provide fast addition.

Now following this in section (2) brief idea about conventional BCD adder is given. In section (3) methodology of proposed 5-input decimal adder is explained with example. In section (4) results of our proposed work after implementation are given.

ANTECEDENT WORK-

Previously 3-input and 4-input decimal adders are proposed. In 3-input decimal adder sum and carry both vectors are used. When sum is generated for inputs this will be added with carry signals output of which gives our result after adding correction bits. Condition for generating Digit generation and Digit propagation signals are given in table below:

Signals	Conditions of the sum in each digit
DG_i [1]	>9
DG_i [2]	>19
DP_i [1]	=9
DP_i [2]	=8
DP_i [3]	=19
DP_i [4]	=18

Table-1 Identifying conditions for generating signals of 3-input adder

In a BCD adder suppose we have two input A(Augends) and B(Addend) are given to decimal BCD adder architecture is shown in figure(1). After using these 1-digit adders with composed of 4 consecutive full adders to add the values of input A and B, the digit adder with correction which is also composed by 4 full adders is used. When result of sum is more than 9 then we add

$(0110)_2$ in each nibble by using correction network.

Augend A_3 A_2 A_1 A_0

Addend B_3 B_2 B_1 B_0

C_{OUT} S_3 S_2 S_1 S_0

Equation for this by k-map is

$CC = C_{out} + S_3 (S_2+S_1)$

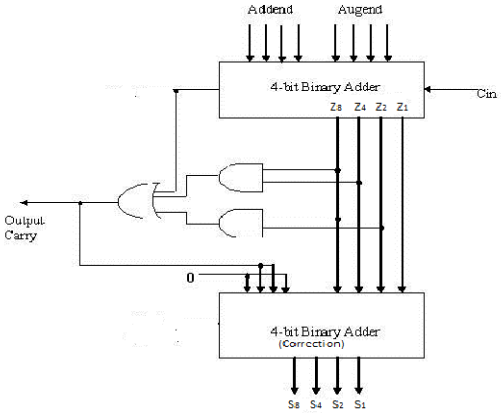

Figure-1 Hardware For 1 Digit BCD Adder

Now if we increase the numbers of input bits numbers of full adders are also increased. So another BCD adder with reduced delay is proposed.

REDUCED DELAY BCD ADDER-

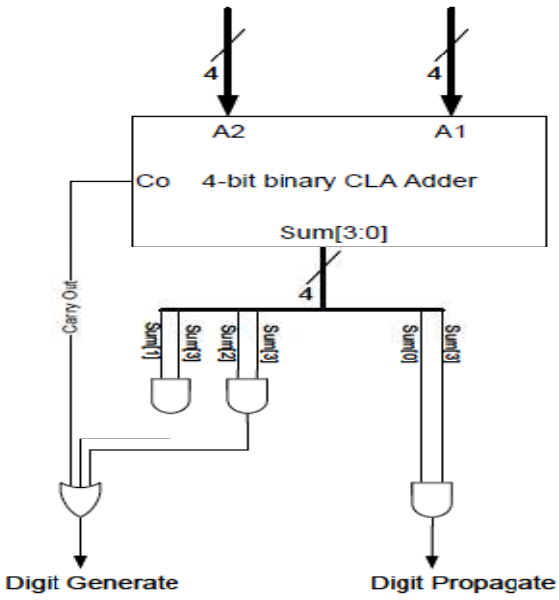

Figure-2 Adder + Analyzer For Producing DG And DP

As we see in figure-2 there are three stages, first stage consist of adder + analyzer which generate sum and two signal DG(Digit generate) and DP(Digit propagate).when the sum of two valid BCD input is greater than 9 it will generate DG. When the sum is equal to 9 signal DP is generated. Equation for this

$C_{out} = DG + DP.C_{in}$

Here + is used for OR logic and . shows AND logic.

PROPOSED AREA EFFICIENT 5-INPUT DECIMAL ADDER-

In our proposed decimal adder as we see in figure 5-input decimal adder consist of three stages and each input is of 4-bits. This input bits are sent to CSA + PG network which produces sum and carry vector with DG and DP signals. In last stage we add sum digits with correction digits by using Carry Save Adder and Carry Look Ahead adder.

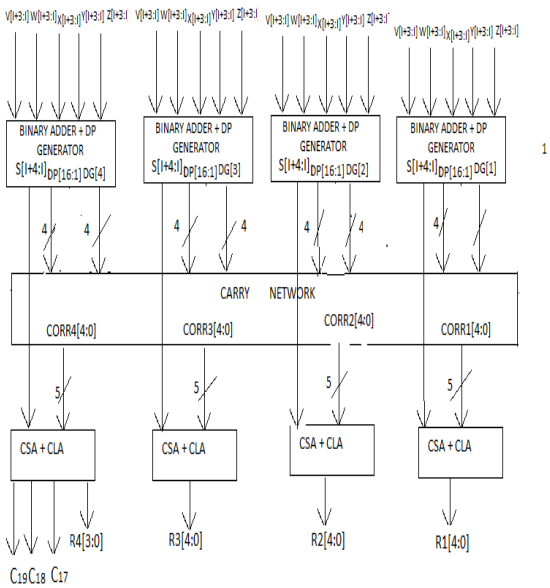

Figure-3 Architechture of Proposed 5-Input Decimal Adder

Condition for Digit generating signal is when sum is greater than 9,19,29 or 39.

When sum of the input digits are equal to 6,7,8,9,16,17,18,19,26,27,28,29,36,37,38,39 it will generate Digit Propagation signal. During addition of input digit carry generated so we add corr[0],corr[1],corr[2],corr[3],corr[4] in output and this will generate our output. When one carry is

generated we add (0110) and (0111) when two carries are generated.

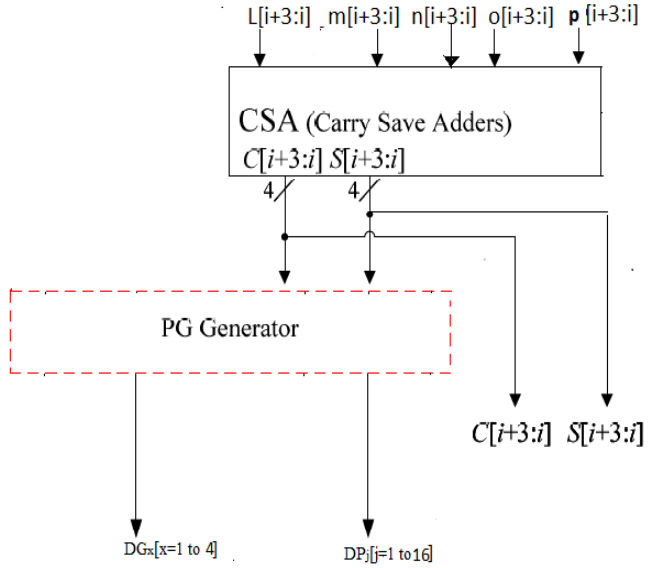

Figure-4 Generation Of DG And DP Signal

Signals	Conditions of producing signals
DG[0]	>9
DG[1]	>19
DG[2]	>29
DG[3]	>39
DP[1]	=6
DP[2]	=7
DP[3]	=8
DP[4]	=9
DP[5]	=16
DP[6]	=17
DP[7]	=18
DP[8]	=19
DP[9]	=26
DP[10]	=27
DP[11]	=28
DP[12]	=29
DP[13]	=36
DP[14]	=37
DP[15]	=38
DP[16]	=39

Table-2 for digit generation and propagation signal identifying conditions in each digit sum

We can understand these conditions with the example-

Input digits are 9234
4876
6542
3435
5678
Output 29765

Digit4	Digit3	Digit2	Digit1	
1001	0010	0011	0100	
0100	1000	0111	0110	
0110	0101	0100	0010	
0011	0100	0011	0101	
+ 0101	0110	0111	1000	
11011	11001	11000	11001	
1	1	1	1	DG [0]
1	1	1	1	DG [1]
0	0	0	0	DG [2]
0	0	0	0	DG [3]
0	0	0	0	DP [1]
0	0	0	0	DP [2]
0	0	0	0	DP[15]

11011	11001	11000	11001	SUM[4]
1110	1110	1110	1100	CORR[4]

COMPARISON OF IMPLEMENTATION RESULT AND CONCLUSION-

In our proposed work for implementation codes of 5-input decimal adder we use verilog module of Xilinx. After synthesize the codes we get delay and its area. Delay for adders can differ if they are synthesized on different modules.

By comparing our results with previously available adders we can conclude that 5-input decimal adder is more area efficient and delay time is less in it. Power consumptions of our adder is less which is calculated by PrimePower. Comparison of delays

among the 3-input and our proposed 5-input decimal adder is shown in table below

Type of adder	Delay(ns)	IO Buffers
5-input(Proposed work)	12.352	99
3-input (Previous work)	11.329	67
3-input(Reduced Delay)	11.016	67
3-input(type-3)	10.499	66

Table-3 Comparisons of Decimal adders

Our proposed work is compared with 3-input and 4-input adder delay in our proposed 5-input decimal adder is a little more but it provide option for addition with large number of input and also in more efficient way in terms of area and delay. So our proposed work is very efficient and useful in higher level addition with increasing number of inputs.

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