Implementation of CMOS Low Dropout (LDO) Voltage Regulator using Frequency Compensation Scheme

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Abstract- The proliferation of battery-powered equipment like cellular, pagers, laptops, camera recorders etc has increased the demand for low-dropout linear regulators (LDO). This paper discusses the different architecture of LDO with different frequency compensation scheme using PMOS dropout element. In frequency compensation scheme of low drop out (LDO) voltage regulators, a Zero generated by the series combination of load capacitor and its Electro Static Resistance (ESR) plays an important role. This frequency compensation tends to be inefficient due to the ESR's value is process and temperature dependent. Experimental results show that the high performance CMOS Low Dropout (LDO) voltage regulator with a robust frequency compensation scheme gives significant stability without relying on ESR. Hence the stability of LDO does not dependent on the ESR. LDO is designed to output constant 3.1v at 200mA. It works on 3.3V power supply and input voltage of 1.21V from band gap reference.

Keywords: LDO Voltage Regulator, ESR, CMOS.

I. Introduction (Low Dropout Voltage Regulator)

As portable electronics constantly find their way into the hands of eager consumers, the demands placed on these products and their circuits are ever increasing. More features and more performance are continuously demanded by consumers. This feature-driven market has brought with it several constraints on the type of circuits utilized in developing these portable devices. Cell-Phones, PDA's, MP3 players and various other portable electronics require different voltage levels to power different architectures that realize the many features within the device. Also power efficiency is main constrain which is related to the battery life time.

Low dropout voltage regulator has gained importance due to demand for power efficient circuits in mobile communications, result of which increased battery life. This is because low dropout voltage regulator has less ground current compare to other linear voltage regulator. A pass element can be PMOS or NMOS. NMOS require a positive drive signal with respect to the output, while PMOS is driven from a negative signal with respect to the input.

II. General Architecture & Performance Metric

2.1 Working of LDO

A **low dropout** or **LDO** regulator is a DC linear voltage regulator which has a very small input-output differential voltage. The main components are a power FET and a differential amplifier (error amplifier). One input of the differential amplifier monitors a percentage of the output, as determined by the resistor ratio of **R1** and **R2**. The second input to the differential amplifier is from a stable voltage reference (band gap reference).

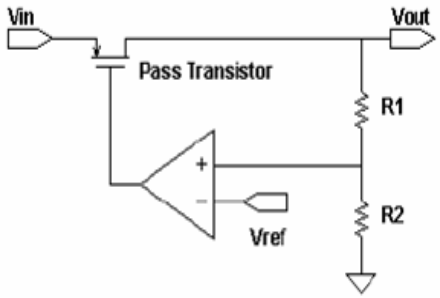


Figure: 2.1 LDO Voltage Regulators

2.1.1 General Architecture of LDO

As a given specification value of CL is 1uF and for maximum load current (200mA) size of pass transistor is large so result of which gate capacitor of pass transistor is also large in the range of few hundred of pF. This value of gate capacitor of pass transistor is large compare to the output capacitor of erroramplifier.

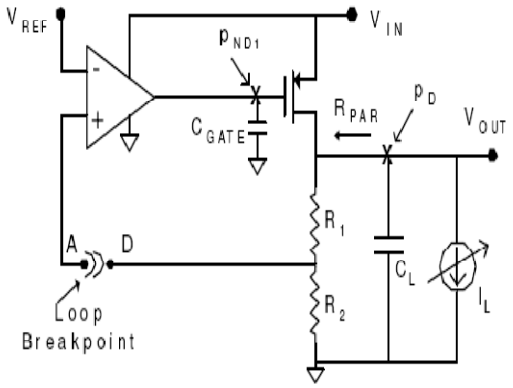


Figure: 2.2 Typical LDO Open Loop Representations.

2.1.3 Different architecture of error amplifier for LDO design

- Miller compensation with P-input error amplifier.
- Folded cascade with P-input error amplifier.
- Without Miller compensation with P-input error amplifier.
- Without Miller compensation with N-input error amplifier.

III. MILLER COMPENSATION WITH P & N INPUT ERROR AMPLIFIER & ITS RESULTS

3.1 LDO with Miller compensation with P-input error amplifier

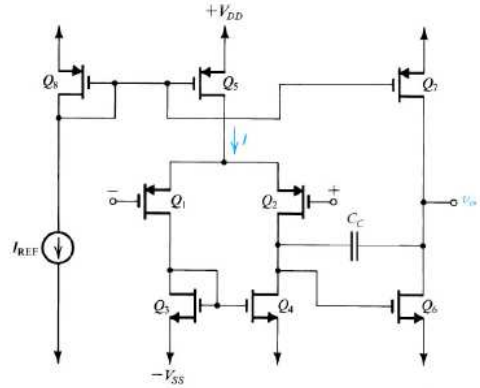
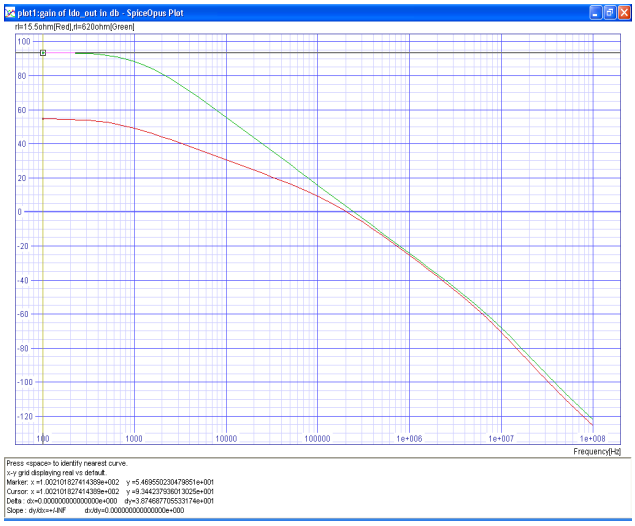
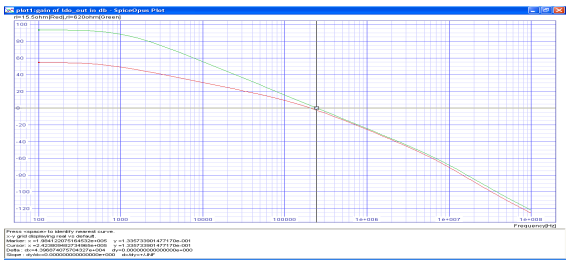


Figure: 3.1. LDO with Miller compensation P-input error amplifier



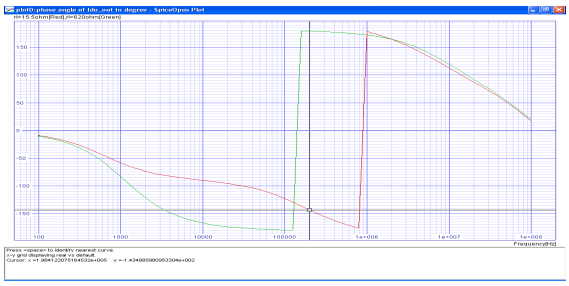
Gain at maximum current (200mA) = 55db.

Gain at minimum current (5mA) = 93db.



UGB at maximum current(200mA) = 1.984e5 Hz

UGB at minimum current(5mA) = 2.4238e5Hz



Phase margin at maximum current (200mA) =37deg

LDO with frequency compensated by ESR:

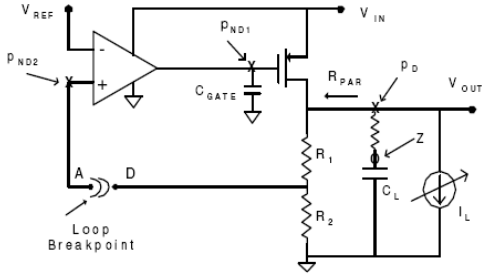
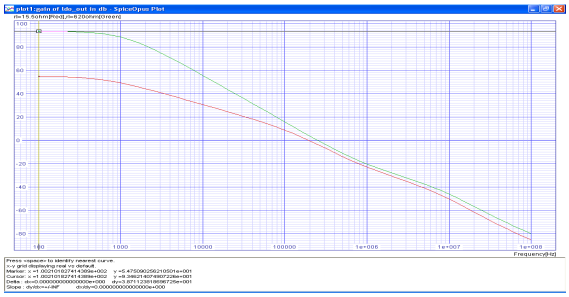


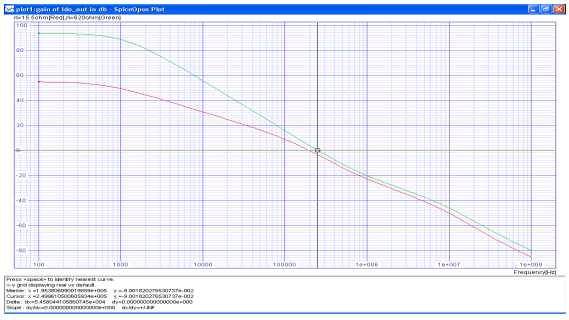
Figure: 3.2 Typical LDO with ESR compensation.

The most common type of LDO commercially available today is one that utilizes the ESR (Electro-Static Resistance) of the output capacitor as a zero generating element in order to compensate the phase loss of one of the two low frequency poles encountered. Fig. 6 shows the typical LDO with the two low frequency poles, a 3rd pole (pND2) at relatively higher frequencies, and the zero used for compensation marked where they occur. The 3rd pole (pND2) is added in order to establish a more realistic system in which the gate capacitance of the error amplifier could potentially bring the pole at that node close to the band of operation of the system. By placing a zero in the open loop transfer function, the phase effect of one of the two low frequency poles will be cancelled and will effectively compensate for the phase margin loss. The zero that is used for phase compensation, when depending on ESR, is given:

Result of LDO with ESR (Electro-Static Resistance) i.e. ESR =0.2ohm

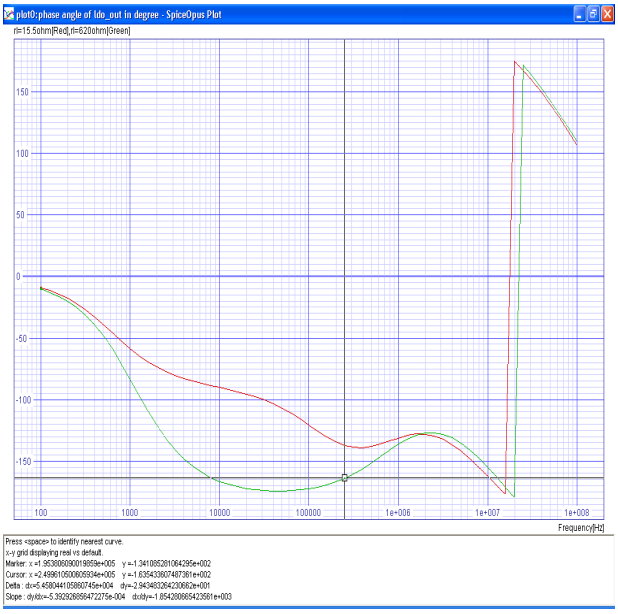


Gain at maximum current (200ma) = 55db
Gain at minimum current (5mA) = 93db



UGB at maximum current (200mA) = 1.9538e5Hz
UGB at minimum current(5mA) = 2.4996e5Hz

Open loop phase margin of LDO



Phase margin at maximum current =46deg
Phase margin at minimum current = 16deg

IV. CONCLUSION

Different architecture of error amplifier behaves differently for stability point of view. As in results shown those P-input error amplifiers give better results than the N-input error amplifier. This is due to two reasons

- Since Vref is 1.21V so PMOS work effectively.
- At the second stage of the error amplifier cascode structure is take place in case of N-input which offer large value of output resistance result of which non dominate pole occur near to UGB. Whereas in P-input error amplifier second stage common source which offer small value of output resistance.

Miller compensation P-input and cascade error amplifier are self compensated so they give significant phase margin at maximum current compare to the other non compensated error amplifiers.

In all type of error amplifier gain, power dissipation, phase margin have trade off point. Frequency compensated by using ESR (Electro Static Resistance) has limitation on the minimum current. Increase in value of output resistance degrade the stability of LDO i.e. phase margin decrease. Also value of ESR is process and temperature dependent.

So to make LDO's stability independent of ESR stability of LDO achieve by robust frequency compensation scheme. In this position of zero move

according to load so it gives better phase margin at no load condition as well as minimum load condition.

V. REFERENCES

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