Design and Performance Analysis of a Double-Tail Comparator for Low-Power Applications

Megha Gupta
M.Tech. VLSI, Suresh Gyan Vihar University Jaipur
Email: megha.gupta0704@gmail.com

Priya Yadav
M.Tech. VLSI, Suresh Gyan Vihar University Jaipur
Email: priya.yadav1393@gmail.com

Abstract*— A comparator is the fundamental building block in most analog-to-digital converters. The need of low-power, area efficient, and high-speed analog-to-digital converters require the use of dynamic regenerative comparators with small die area to maximize the speed and power efficiency. Designing of high speed comparators is more difficult when the supply voltage is smaller due to the use of large transistors to compensate the reduction of supply voltage which results in increase in die area, delay and power of the comparator. In this paper, an analysis on the delay and power consumption of the dynamic comparators will be presented. Based on the presented analysis, a new fully double-tail comparator using positive feedback is proposed, in which the conventional double-tail comparator is modified for lesser power consumption and high speed even in small supply voltages. The proposed topology is based on placing two cross coupled control transistors along the input side of the double-tail comparator. This cross coupled control transistors strengthens the positive feedback during the regeneration which reduces the delay time. Addition to that switching transistor is added to reduce the power dissipation. Circuit simulation results in a 0.18-μm CMOS technology confirm the analysis results. It is shown that in the proposed double-tail comparator both the power consumption and delay time is significantly reduced in comparison with all other dynamic comparators.

Index Terms*— Double-tail comparator, dynamic latch comparator, high speed analog-to-digital converters (ADCs), low-power analog design.

I. INTRODUCTION

Comparator is one of the fundamental building blocks in most analog to digital converters (ADCs). High speed flash ADCs, require high speed, low power and small chip area. Comparators are known as 1-bit analog to digital converter and hence they are mostly used in large abundance in A/D converter.

A comparator is same as that like of an operational amplifier in which they have two inputs (inverting and non-inverting) and an output. The function of a CMOS comparator is to compare an input signal with a reference signal which produces a binary output signal. Comparator uses back-to-back cross-coupled inverters to convert a small input voltage-difference to digital output in a short period of time.

It is more challenging to design a high speed comparator with a small supply voltage [1]. The performance of the comparator plays an important role in realization of high integration, low power, low cost and good design. Mismatch in the load capacitors can lead to offset in the comparator it will consume more power [2]. The high speed comparators will lead the supply voltage becomes larger [3], [4]. Many techniques, such as supply boosting methods [6], [7], techniques employing body-driven transistors [8], [9], current-mode design [10] and those using dual-oxide processes, which can handle higher supply voltages have been developed to meet the low-voltage design challenges. These are effective techniques, but they introduce reliability issues especially in UDSM CMOS technologies. The fastest and more power efficient comparators generate more kickback noise. Minimizing kickback noise is the complex process and it will require more power [11].

In [12]–[14], additional circuitry is added to the conventional dynamic comparator to enhance the comparator speed in low supply voltages. The proposed comparator of [12] works down to a supply voltage of 0.5 V with a maximum clock frequency of 600 MHz and consumes 18 μW. Despite the effectiveness of this approach, the effect of component mismatch in the additional circuitry on the performance of the comparator should be considered. The structure of double-tail dynamic comparator first proposed in [15] is based on designing a separate input and cross-coupled stage. This separation enables fast operation over a wide common-mode and supply voltage range. In this paper, the delay analysis of dynamic comparators has been presented for various architectures. Furthermore, based on the double-tail structure proposed in [15], a new dynamic comparator is presented, which does not require boosted voltage or stacking of too many transistors. Merely by adding a few minimum-size transistors to the conventional double-tail dynamic comparator, latch delay time is profoundly reduced. This modification also results in considerable power savings when compared to the conventional dynamic comparator and double-tail comparator.

The rest of this paper is organized as follows. Section II investigates the operation of the dynamic comparators and the pros and cons of each structure are discussed. The proposed comparator is presented in Section III. Simulation results are addressed in Section IV, followed by conclusions in Section V.

II. DYNAMIC COMPARATOR

Conventional dynamic [16] and double-tail comparators [15] are clocked regenerative comparators which are useful in high speed ADCs like flash ADC because of their fast decision making capability due to strong feedback loop in the regenerative latch. Recently, many comprehensive analysis have been presented, which investigate the performance of these comparators from different aspects, such as noise, offset and random decision errors, and kick-back noise. In this section, a comprehensive delay analysis is presented; the delay time of two common structures, i.e., conventional dynamic comparator and conventional double-tail comparator are analyzed, based on which the proposed comparator will be presented.

A. Conventional Dynamic Comparator

The schematic diagram of the conventional dynamic comparator is shown in Fig. 1. It consists of *reset phase* and *comparison phase* of operation in it.

During the reset phase, when CLK = 0 and M_{tail} is off, reset transistors (M7–M8) pull both output nodes Out_n and Out_p to V_{DD} to define a start condition and to have a valid logical level during reset.

In the comparison phase, when CLK = V_{DD}, transistors M7 and M8 are off, and M_{tail} is on. Output voltages (Out_p, Out_n), which had been pre-charged to V_{DD}, start to discharge with different discharging rates depending on the corresponding input voltage (INN/INP). Assuming the case where $V_{INP} > V_{INP}$, Out_p discharges faster than Out_n, hence when Out_p (discharged by transistor M2 drain current), falls down to $V_{DD}–|V_{thp}|$ before Out_n (discharged by transistor M1 drain current), the corresponding PMOS transistor (M5) will turn on initiating the latch regeneration caused by back-to-back inverters (M3, M5 and M4, M6). Thus, Out_n pulls to V_{DD} and Out_p discharges to ground. If $V_{INP} < V_{INN}$, the circuits works vice versa. In case, the voltage at node INP is bigger than INN (i.e., $V_{INP} > V_{INN}$), the drain current of transistor M2 (I_2) causes faster discharge of Out_p node compared to the Out_n node, which is driven by M1 with smaller current.

This dynamic comparator has the advantages of high input impedance, rail to rail output swing, no static power consumption and good robustness against noise and mismatch. The disadvantage is due to several stacked transistors, a sufficiently high supply voltage is needed for a proper delay time. Another drawback is the only one current path, via tail transistor M_{tail}, which defines the current for both the differential amplifier and the latch.

The delay of this comparator is comprised of two time delays, t_0 and t_{latch}. The delay t_0 represents the capacitive discharge of the load capacitance C_L until the first p-channel transistor (M5/M6) turns on and t_{latch} is the latching delay of two cross-coupled inverters. The total delay of conventional dynamic comparator is given as:

$$t_{delay} = t_0 + t_{latch} = 2\frac{C_L|V_{thp}|}{I_{tail}} + \frac{C_L}{g_{m,eff}}.ln\left(\frac{V_{DD}}{4\,|V_{thp}|\Delta V_{in}}\sqrt{\frac{I_{tail}}{\beta_{1,2}}}\right). \quad (1)$$

where $g_{m,eff}$ is the effective transconductance of the back-to-back inverters, $\beta_{1,2}$ is the input transistor's current

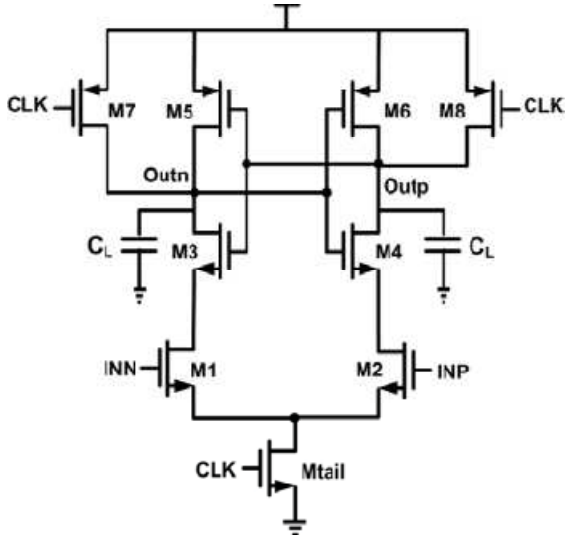

Fig.1. Schematic diagram of the conventional dynamic comparator.

factor, C_L is the comparator load capacitance, I_{tail} is the bias current and ΔV_{in} is the input difference voltage.

B. Conventional Double Tail Dynamic Comparator

The schematic diagram of the Conventional Double-Tail Comparator is shown in Fig. 2. A conventional double-tail comparator has less stacking and therefore can operate at lower supply voltages compared to the conventional dynamic comparator. The double-tail enables both a large current in the latching stage and wider M_{tail2}, for fast latching independent of the input common-mode voltage and a small current in the input stage.

The operation of this comparator is, During reset phase (CLK = 0, M_{tail1}, and M_{tail2} are off), transistors M3-M4 pre-charge f_n and f_p nodes to V_{DD}, which in turn causes transistors MR1 and MR2 to discharge the output nodes to ground.

During decision-making phase (CLK = V_{DD}, M_{tail1} and M_{tail2} turn on), M3-M4 turn off and voltages at nodes f_n and f_p start to drop with the rate defined by $I_{Mtail1}/C_{fn(p)}$ and on top of this, an input-dependent differential voltage $\Delta V_{fn(p)}$ will build up. The intermediate stage formed by MR1 and MR2 passes $\Delta V_{fn(p)}$ to the cross coupled inverters and also provides a good shielding between input and output, resulting in reduced value of kickback noise. The voltage difference at the first stage outputs ($\Delta V_{fn/fp}$) at time t_0 has a profound effect on latch initial differential output voltage (ΔV_0) and consequently on the latch delay. Therefore, increasing it would profoundly reduce the delay of the comparator. In this comparator, both intermediate stage transistors will be finally cut-off, (since f_n and f_p nodes both discharge to the ground), hence they do not play any role in improving the effective transconductance of the latch. Besides, during reset phase, these nodes have to be charged from ground to V_{DD}, which means power consumption. It has high peak transient noise voltage at the

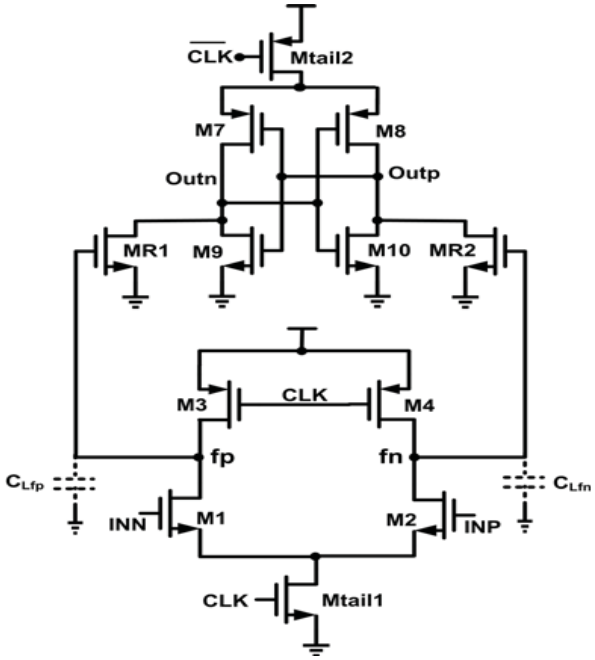

Fig. 2. Schematic diagram of conventional double-tail comparator.

regeneration time and low kickback noise voltage. It has high energy per conversion and input referred offset voltage than the conventional Dynamic comparator. This Double Tail comparator contains two Mtail transistors i.e. two current path in it. So, it will increase the performance of the comparator.

The delay of this comparator also comprises two main parts, t0 and tlatch. The delay t0 represents the capacitive charging of the load capacitance CLout (at the latch stage output nodes) until the first n-channel transistor (M9/M10) turns on, after which the latch regeneration starts. Hence the total delay of conventional double tail comparator is given as:

$$t_{delay} = t_0 + t_{latch} = 2\frac{C_{Lout}V_{thn}}{I_{tail2}} + \frac{C_{Lout}}{g_{m,eff}} . ln\left(\frac{V_{DD}.I_{tail2}^2.C_{L,fn(p)}}{8V_{thn}^2.C_{Lout}g_{mR1,2}g_{m1,2}\Delta V_{in}}\right). \quad (2)$$

where gmR1,2 is the transconductance of the intermediate stage transistors (MR1 and MR2) and Itail2 is the latch tail current.

III. PROPOSED DOUBLE-TAIL DYNAMIC COMPARATOR

Fig. 3 demonstrates the schematic diagram of the proposed dynamic double-tail comparator. Due to the better performance of double-tail architecture in low-voltage applications, the proposed comparator is designed based on the double-tail structure. The main idea of the proposed comparator is to increase ΔVfn/fp in order to increase the latch regeneration speed. For this purpose, two control transistors (Mc1 and Mc2) have been added to the first stage in parallel to M3/M4 transistors but in a cross-coupled manner [see Fig. 5(a)].

The operation of the proposed comparator is as follows. During reset phase (CLK = 0, Mtail1 and Mtail2 are off, avoiding static power), M3 and M4 pulls both fn and fp nodes to VDD, hence transistor Mc1 and Mc2 are cut off. Intermediate stage transistors, MR1 and MR2, reset both latch outputs to ground. During decision-making phase (CLK = VDD, Mtail1, and Mtail2 are on), transistors M3 and M4 turn off. Furthermore, at the beginning of this phase, the control transistors are still off (since fn and fp are about VDD). Thus, fn and fp start to drop with different rates according to the input voltages. Suppose VINP > VINN, thus fn drops faster than fp, (since M2 provides more current than M1). As long as fn continues falling, the corresponding pMOS control transistor (Mc1 in this case) starts to turn on, pulling fp node back to the VDD; so another control transistor (Mc2) remains off, allowing fn to be discharged completely. In other words, unlike conventional double-tail dynamic comparator, in which ΔVfn/fp is just a function of input transistor transconductance and input voltage difference, in the proposed structure as soon as the comparator detects that for instance node fn discharges faster, a pMOS transistor (Mc1) turns on, pulling the other node fp back to the VDD. Therefore by the time passing, the difference between fn and fp (ΔVfn/fp) increases in an exponential manner, leading to the reduction of latch regeneration time. Despite the effectiveness of the proposed idea, one of the points which should be considered is that in this circuit, when one of the control transistors (e.g., Mc1) turns on, a current from VDD is drawn to the ground via input and tail transistor (e.g., Mc1, M1, and Mtail1), resulting in static power consumption.

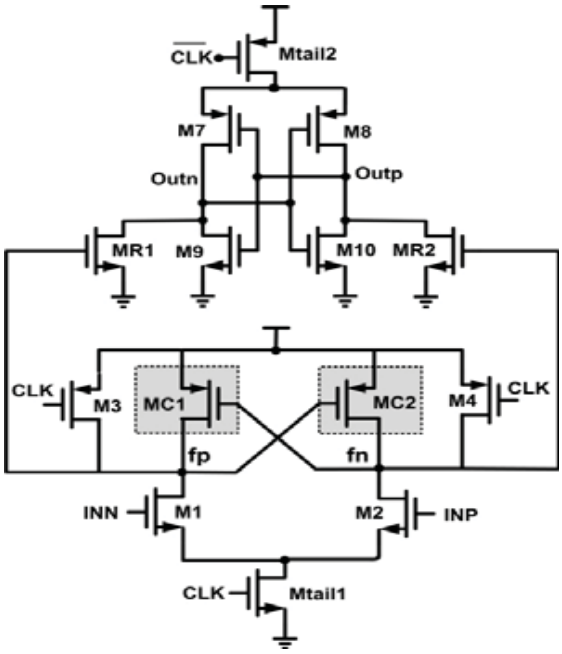

Fig. 3(a). Schematic diagram of the proposed dynamic comparator (Main idea)

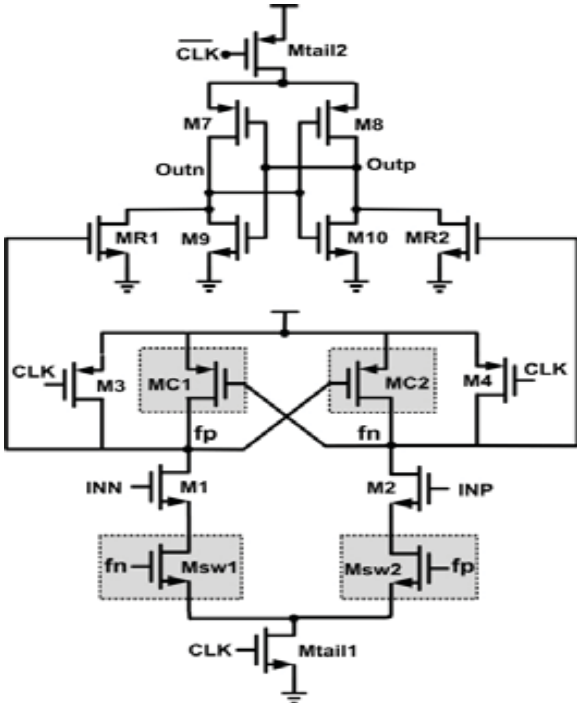

Fig. 3(b). Schematic diagram of the proposed dynamic comparator (Final Structure)

To overcome this issue, two nMOS switches are used below the input transistors [Msw1 and Msw2, as shown in Fig. 3(b)]. At the beginning of the decision making phase, due to the fact that both f_n and f_p nodes have been pre-charged to V_{DD} (during the reset phase), both switches are closed and f_n and f_p start to drop with different discharging rates. As soon as the comparator detects that one of the f_n/f_p nodes is discharging faster, control transistors will act in a way to increase their voltage difference.

Suppose that f_p is pulling up to the V_{DD} and f_n should be discharged completely, hence the switch in the charging path of f_p will be opened (in order to prevent any current drawn from V_{DD}) but the other switch connected to f_n will be closed to allow the complete discharge of f_n node. In other words, the operation of the control transistors with the switches emulates the operation of the latch.

The novelty of the design is that it has high speed compared to the conventional double-tail dynamic comparator due to increament in the initial output voltage difference (ΔV_0) at the beginning of the regeneration (t_0) and effective transconductance ($g_{m,eff}$). In the proposed comparator, the energy per conversion is also reduced. The total delay of the proposed comparator is given as:

$$t_{delay} = t_0 + t_{latch} = 2\frac{C_{Lout}\,V_{thn}}{I_{tail2}} + \frac{C_{Lout}}{g_{m,eff} + g_{mR1,2}} . ln\left(\frac{V_{DD}/2}{4V_{thn}|V_{thp}|\frac{g_{mR1,2}g_{m1,2}\Delta V_{in}}{I_{tail2}\,I_{tail1}}exp\left(\frac{G_{m,eff1}\cdot t_0}{C_{L,fn(p)}}\right)}\right) \quad (3)$$

IV. RESULT ANALYSIS

Transient simulation of the conventional dynamic comparator [16], conventional double-tail comparator [15] and proposed double-tail comparator were performed with 180nm sub-micron technology with V_{DD}=0.8V. Here the results of the existing comparators in terms of delay and power are shown in TABLE I.

TABLE I. SUMMARY OF THE COMPARATOR PERFORMANCE

Comparator	Delay	Power
Conventional Dynamic Comparator	7 ns	66 µW
Conventional Double-Tail Comparator	7.5 ns	15 µW
Proposed Double-Tail Comparator	7.3ns	12 µW

V. CONCLUSION

In this paper, a delay analysis for clocked dynamic comparators is presented. Two basic structures of conventional dynamic comparator and conventional double-tail dynamic comparators were analyzed. Based on that, a new dynamic comparator with low-voltage low-power capability was proposed in order to improve the performance of the comparator. The simulation results in 0.18-µm CMOS technology confirmed that the delay and power consumption of the proposed comparator is reduced to a great extent in comparison with the conventional dynamic comparator and double-tail comparator.

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