

Clock Gating For Dynamic Power Reduction In Synchronous Circuits

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Abstract – A method to reduce power dissipation by automatically synthesizing gated-clocks is presented for low power VLSI (very large scale integration) circuit design. Clock power is a major source of dynamic power consumed in synchronous circuits because the clock is fed to most of the circuit blocks, and the clock switches every cycle. Thus the total clock power is a substantial component of total power dissipation in a digital circuit. Clock-gating is a well-known technique to reduce clock power. In clock gating clock to an idle block is disabled. Thus significant amount of power consumption is reduced by employing clock gating. In this method a 4-bit synchronous counter is designed using clock gating. A technique for clock gating is also presented, which generates a derived clock synchronous with the master clock. Design examples using gated clocks are provided next. Simulation is performed on Xilinx ISE design tool. Result shows that the clock gating technique significantly improves total dynamic power consumption. It is observed that approximately 11% of dynamic power is saved.

Index Terms—Clock gating, low power, synchronous counter.

I. INTRODUCTION

The sequential circuits in a system are considered major contributors to the power dissipation since one input of sequential circuits is the clock, which is the only signal that switches all the time. In addition, the clock signal tends to be highly loaded. To distribute the clock and control the clock skew, one needs to construct a clock network (often a clock tree) with clock buffers. All of this adds to the capacitance of the clock net. Recent studies indicate that the clock signals in digital computers consume a large (15–45%) percentage of the system power [1]. Thus, the circuit power can be greatly reduced by reducing the clock power dissipation. In recent years, the demand for power-sensitive designs has grown significantly. This tremendous demand has mainly been due to the fast growth of battery-operated portable applications such as notebook and laptop computers, personal digital assistants, cellular iphones, and other portable communication devices. Semiconductor devices are aggressively scaled each technology generation to

achieve high-performance and high integration density. Due to increased density of transistors in a die and higher frequencies of operation, the power consumption in a die is increasing every technology generation. Supply voltage is scaled to maintain the power consumption within limit. However, scaling of supply voltage is limited by the high-performance requirement. Hence, the scaling of supply voltage only may not be sufficient to maintain the power density within limit, which is required for power-sensitive applications. Circuit technique and system-level techniques are also required along with supply voltage scaling to achieve low-power designs. In the nano-meter regime, a significant portion of the total power consumption in high performance digital circuits is due to leakage currents. Because high-performance systems are constrained to a predefined power budget, the leakage power reduces the available power, impacting performance.

In VLSI circuit clock signal is used for the synchronization of active components. Clock power is a major component of power mainly because the clock is fed to most of the circuit blocks, and the clock switches every cycle. Thus the total clock power is a substantial component of total power dissipation in a digital circuit [4]. Clock-gating is a well-known technique to reduce clock power. In a sequential circuit individual blocks usage depends on application, not all the blocks are used simultaneously, giving rise to dynamic power reduction opportunity. By clock gating technique, clock to an idle portion is disabled, thus avoiding power dissipation due to unnecessary charging and discharging of the unused circuit.

In clock gating clock is selectively stopped for a portion of circuit which is not performing any active computation [3]. Local clocks that are conditionally enabled are called gated clocks, because a signal from the environment is used to gate the global clock signal [2]. In this paper a CMOS clock gated synchronous counter has been proposed. Section II explains various types of power dissipated in a synchronous circuit. In section III previous work in the field of clock gating has been discussed in section IV clock gating technique is given for a synchronous latch, and in section V a synchronous counter is designed employing gated

clock. A comparison of gated and non gated clock circuit is also given in this section.

This eliminates the additional skew between the master clock and the derived clock. Thus, the designed sequential circuit is a synchronous one. Finally, we present circuit simulation results to prove the quality of the derived clock and its ability to reduce power dissipation in the circuit.

II. SOURCES OF POWER CONSUMPTION IN DIGITAL CMOS CIRCUITS

There are four components which contribute to the average power consumption P_{avg} of a digital CMOS circuit:

$$P_{avg} = P_{leakage} + P_{short-circuit} + P_{dynamic} + P_{static};$$

Where ,

Dynamic(Switching) power $P = CV^2f\alpha$

Short circuit power $P = I_{short-circuit}V$

Leakage power $P = I_{leakage}V$

Static power $P = I_{static}V$

α : switching activity factor

P_{avg} is the average power dissipation, $P_{dynamic}$ is the dynamic power dissipation due to switching of transistors, $P_{short-circuit}$ is the short-circuit current power dissipation when there is a direct current path from power supply down to ground, $P_{leakage}$ is the power dissipation due to leakage currents, P_{static} and is the static power dissipation.

a) Static power

Static power is the power dissipated by a gate when it is not switching that is, when it is inactive or static. Ideally, CMOS (Complementary Metal Oxide Semiconductor) circuits dissipate no static (DC) power since in the steady state there is no direct path from V_{DD} to ground. This scenario can never be realized in practice, since in reality the MOS transistor is not a perfect switch. There will always be leakage currents, sub threshold currents, and substrate injection currents, which give rise to the static component of power dissipation. The largest percentage of static power results from source-to-drain sub threshold voltage, which is caused by reduced threshold voltages that prevent the gate from completely turning off.

b) Dynamic power

The dynamic power, also called switching or capacitive power, is by far the most significant component and accounts for approximately 80% of the overall power consumption. Switching power is dissipated when the capacitive load $C(y)$ of a CMOS gate is being charged by the current I_{switch} through the p-device to make a transition from ground to V_{DD} . The energy required for this transition is $C(y)V_{DD}^2$. Power-consuming transitions occur at a frequency $1/2\alpha(y)f_{clk}$ proportional to the clock frequency f_{clk} , where $\alpha(y)$ is 2

the probability of signal y to make a '0' to '1' or '1' to '0' transition.

The total switching power of a circuit is therefore:

$$P_{switching} = \frac{1}{2} f_{clk} V_{DD}^2 \sum \alpha(Y) C(y)$$

above Eq. shows that the switching power increases linearly with the clock frequency. To reduce the switching power even for increasing clock frequency, we therefore have the following opportunities:

Since the supply voltage V_{DD} influences the $P_{switching}$ quadratically, it is most effective to reduce V_{DD} . However, a lower supply voltage also results in slower switching speed and therefore degrades performance of the circuit accordingly. The relationship between delay, i.e. clock frequency, can be expressed as follows:

$$f_{clk} \propto 0.7 - V_t / V_{DD}$$

Where, V_t is the threshold voltage of the given technology.

To reduce the switched capacitance $P_{signal} = \alpha(y)C(y)$ of the circuit, we can decrease the switching activity of a signal y by appropriately restructuring and/or modifying the fanin logic feeding signal y . Alternatively, we can reduce the actual physical capacitance $C(y)$ to be switched by a signal y . $C(y)$ depends on the output capacitance of the corresponding gate, the wiring capacitance and the gate capacitances of the fanout gates. All of these are in turn dependent on the technology used. However, it is important to note that wiring length does not scale proportionally to the feature sizes of the underlying technology, but that its scaling behavior depends on the wire locality. For global wires, capacitance typically grows with technology scaling.

Therefore, global wiring capacitance is becoming a dominating parameter in $C(y)$ for deep-submicron technologies. To reduce power, we therefore have to pay special attention to global wiring capacitances.

III. DESCRIPTION FOR CLOCK BEHAVIOR AND CLOCK-GATING

In a synchronous system, a flip flop is triggered by a certain directional transition of a clock signal. For the clock to be another signal rather than the master clock, it must offer the same directional transition to trigger the flip flop and it must be in step with the master clock. Clock gating is an effective way of reducing the dynamic power dissipation in digital circuits. In a typical synchronous circuit such as the general purpose microprocessor, only a portion of

the circuit is active at any given time. Hence, by shutting down the idle portion of the circuit, the unnecessary power consumption can be prevented. One of the ways to achieve this is by masking the clock that goes to the idle portion of the circuit.

Clock power is a major component of power mainly because the clock is fed to most of the circuit blocks, and the clock switches every cycle. Thus the total clock power is a substantial component of total power dissipation in a digital circuit. By clock gating technique, clock to an idle portion is disabled, thus avoiding power dissipation due to unnecessary charging and discharging of the

original clock since it toggles for every clock cycle. In order to mask clock signal to flip flops at higher bit positions during their idle states, local clock signals are derived. These signals are GC1, GC2, and GC3 as shown in Fig. 4 (b).

Power calculation is done by Xilinx XPower analyser. Clock frequency of 50 MHz is used for simulation. Simulation results shows above 11% of dynamic power saving.

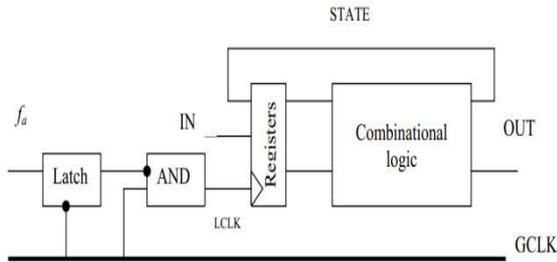


Fig. 1. Schematic diagram of gated clock design

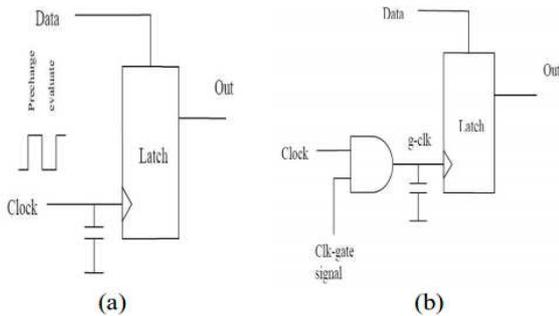


Fig. 2 (a) Synchronous latch without clock gating, (b) Gated clock implementation in latch.

unused circuit. In clock gating clock is selectively stopped for a portion of circuit which is not performing any active computation. This is done by using a signal from the environment. An example of gated clock is shown in figure.

IV. DESIGN OF SYNCHRONOUS CIRCUITS BASED ON DERIVED CLOCK

With the help of a 4 bit binary synchronous up counter using j-k flip-flop as design example in this paper. In a 4 bit up counter LSB bit toggles for every clock cycle, whereas higher bits toggles only if all the lower bits are high as shown in truth table.

A 4 bit synchronous up counter is shown in the figure. Single clock is applied to all the flip flops of a synchronous counter. Since the MSB flip flop of the counter is idle most of the time, an unnecessary clock power is consumed by the circuit. Therefore to reduce clock power, clock signal to the flip flops at higher bit positions can be masked for the idle duration. In this example of gated clock circuit, clock signal is divided into four parts. LSB flip flop is given

Output			
Q(3)	Q(2)	Q(1)	Q(0)
0	0	0	0
0	0	0	1
0	0	1	0
0	0	1	1
0	1	0	0
0	1	0	1
0	1	1	0
0	1	1	1
1	0	0	0
1	0	0	1
1	0	1	0
1	0	1	1
1	1	0	0
1	1	0	1
1	1	1	0
1	1	1	1

Fig. 3 Truth table

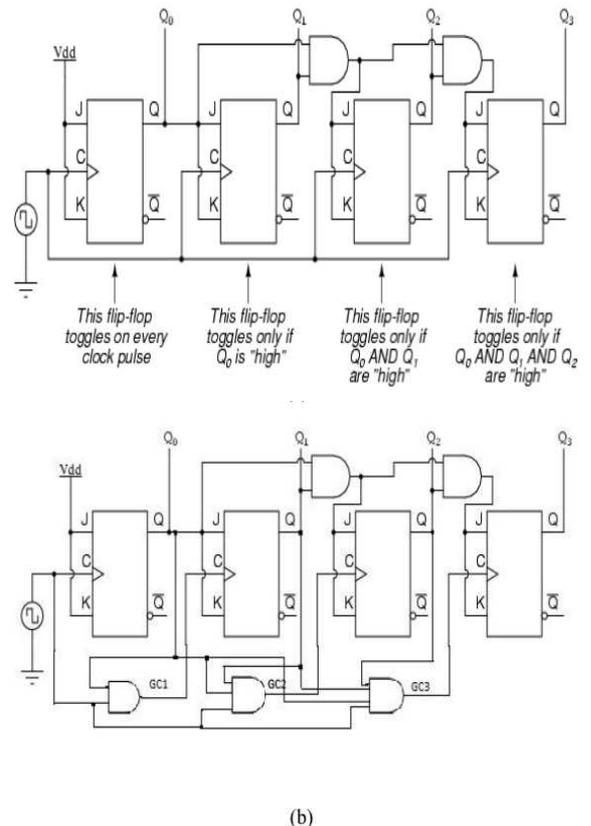


Fig. 4 (a) Synchronous up counter without gated clock (b) Counter using gated clock.

On chip	Power(w)	Used	Available	Utilization(%)
Clocks	0.001	1
Logic	0.000	4	364200	0
Signals	0.000	9
Ios	0.008	10	600	2
Leakage	0.529			
Total	0.538			
Thermal properties	Effective	TJA(C/W)	Max ambient@	Junction temp@
	1.4		84.3	25.7

Supply summary		Total current(A)	Dynamic current (A)	Quiescent current(A)
Source	Voltage			
vccint	1.000	0.363	0.001	0.362
vccaux	1.800	0.093	0.000	0.093
Vcco18	1.800	0.004	0.004	0.000
vccbram	1.000	0.002	0.000	0.002

a)

b)

Fig. 5. Data used in Xilinx XPower analyser for (a) non clock gated and (b) clock gated counter.

V. CONCLUSION

For both high-performance and portable applications power consumption has become a critical design parameter. Therefore, power has to be reduced at all stages of the design flow, from system/algorithmic level down to the physical level. In this paper a simple method to reduce dynamic power consumption of sequential circuit is introduced.

The proposed scheme is based on clock gating technique and gate based clock gating is used in design example. Result shows that clock gating technique significantly reduces the dynamic power consumption. Dynamic power of gated clock counter is 8mW whereas without gated clock the dynamic power is 9mW.

In conclusion clock gating technique significantly reduces dynamic power of sequential circuit, but may increase number of logics, and hence area will increase.

VI. FUTURE WORK

Because of the fact that process variability is increasing as a consequence of the scaling of the CMOS technologies, further research on circuit techniques to reduce the effect of the power parameter variability is needed. Based on analyzing the relation in clock gating with the d-flip-flop, we then presented a new technique for reducing power in

synchronous circuit. Circuit simulation proved the quality of the new derived clock and its capability to reduce power dissipation. More work is needed to develop a systematic design procedure and an algorithm for realizing the proposed design principles for clock gating in large sequential circuits.

VII. REFERENCES

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On chip	Power(w)	Used	Available	Utilization(%)
Clocks	0.001	4
Logic	0.000	9	364200	0
Signals	0.000	11
Ios	0.007	10	600	2
Leakage	1.000 0.529			
Total	1.800 0.537			
Thermal properties	Effective	TJA(C/W)	Max ambient@	Junction temp@
	1.4		84.3	25.7

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