Low area and delay based 16 bit Microcontroller designing by VHDL .

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Abstract

We are working on a paper which name 16 bit microcontroller designing By VHDL with better performance. This paper is based on a new low power designed technique that allows us to solving most of the problems. By use of only pipelining we can implement more complex circuits of digital electronics .this method is beneficial for fast low power circuits by use of reduce number of transistors.

Introduction

We are reducing the delay of our new microcontroller by use VHDL language. In this thesis we will work at delay and power consumption part . We reusing the delay up 6.00ns . Basicaly delay will depends on a total number of Lut's . If we will reduce the total number of LUT the n it will automatically reduce the delay .

After reduce the delay we are increasing the speed of a controller. Actually if speed increase will found in IC then the performance of any circuit in which that IC is using also increase . Dur o this if we will use a low delay and power consumption controller then it will increase the performance of the circuit in which it is using .

```
Data Path: outputreg_11 to outputreg<11>
                                   Gate     Net
  Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
  ----------------------------------------  ------------
   LD:G->Q              2   0.727   0.465  outputreg_11 (outputreg_11)
   OBUF:I->O                5.412          outputreg_11_OBUF (outputreg<11>)
  ----------------------------------------
  Total                    6.604ns (6.139ns logic, 0.465ns route)
                                   (93.0% logic, 7.0% route)
```

We are using a parallel pipe lining for better performance .

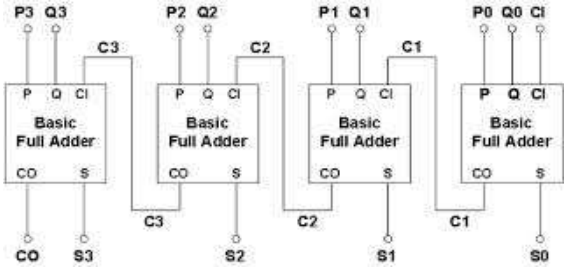
Pipelining:-

Pipelining is a method in which we will transfer all the data parallel way so that no

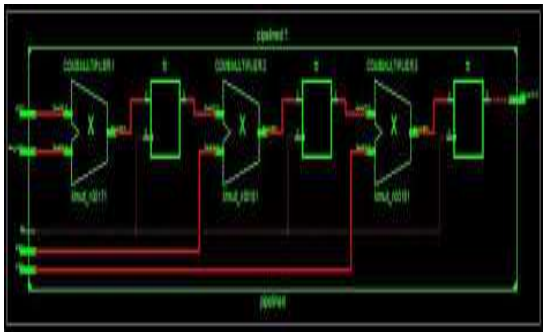
one data will wait for the competition of any other it will goes parallel . In this technique we will transfer data to destination in parallel way . Regarding this all the data will go parallel no one will wait for the completion of any other process.

There are two images in first image we can see that there is using full adder but the output of first full adder is going to another full adder when the first full adder will not give the result till that the second output will not give the answer. Regarding this all the remaining three full adder is also connected. So they will get delay due to connection in series if we will connect this by pipelining then they will connect they will not work serially and they will work in deviously.

In the second image we are using pipelining regarding this the output of first will be goes in second but second will not wait for complete of first block. All the lock will work parallel so data will go parley and it will be in low delay and power consumption area .



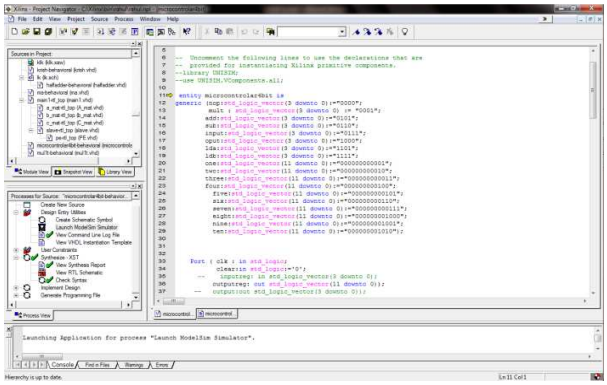
Serially full adder connection



Example of pipelining

We are performing all the coding at XILINX project navigator 6.1 with installed modelsim 5.4 .

Xilinx is a software where we will perform all the coding at VHDL and verilog . Modelsim is used for generate the waveforms. We can used modelsim for waveform generation .



VHDL software image

Xilinx is using for check delay , power consumption , area, number of LUT's check We can perform all the VHDL codes at Xilinx software . We are using Xilinx for design microcontroller. In the block of

synthesis report we can check the delay of controller .

we are designing mnemonics in generic part. Mnemonics are the opcode by which we can perform many operations. In microcontroller we will perform all the operations by mnemonics . We have provide the particular address for store the mnemonics .

nop:std_logic_vector(3 downto 0):="0000";
mult:std_logic_vector(3downto0) := "0001";

add:std_logic_vector(3 downto 0):="0101";

sub:std_logic_vector(3 downto 0):="0110";

input:std_logic_vector(3downto0):="0111";
oput:std_logic_vector(3 downto 0):="1000";
lda:std_logic_vector(3 downto 0):="1101";

ldb:std_logic_vector(3 downto 0):="1111";

There are total eight mnemonics which is using in microcontroller .

NOP :- no operation

MULT :- For multiplication

ADD :- For addition

SUB :- subtraction

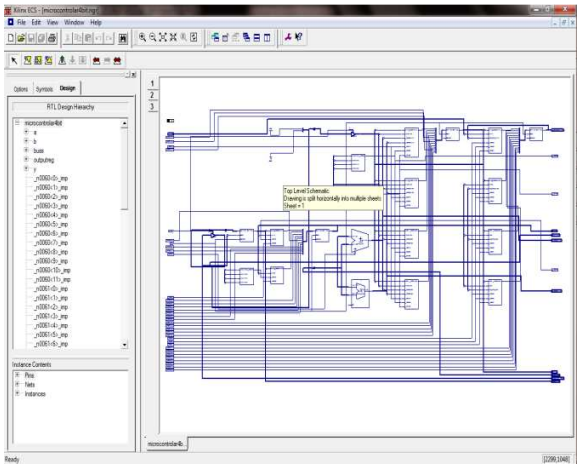
Input :- for transfer input

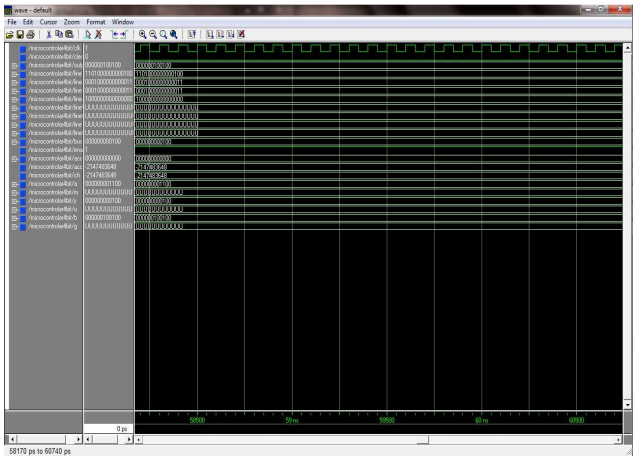
Output :- take a output

LDA :- load in accumulator A

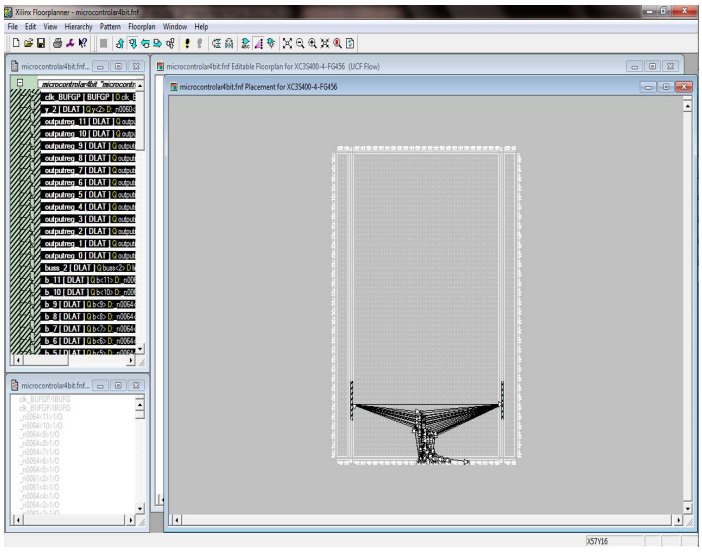
LDB :- Load in accumulator B

Result :-





Waveform



Floor planer

Conclusion :- We have design a new microcontroller in which we have designed own mnemonics . We have a authority to give any name of mnemonics because we are designing a self depend new microcontroller. This controller user has a flexibility that he/she can perform any coding in this controller. For example we want to perform 3 * 3 * 3 then we can write a program in assembly language controller gives a output. User can change the program if user want to perform 3-2+1 then user can perform this. For perform user want to write a program in assembly language and then program will be performed.

In this thesis we worked on parameters of controller. We have a lots of problem in delay . Suppose we are making a program for led blinking but when we implement it at hardware due to this there will be a some delay which will be coming in hardware. That delay is non removable . Because this is a delay of IC . We never remove the delay of IC. Microcontroller is using mostly in every circuit of electronics. So if we reduce the parameters of controller then that will be shows that we are increasing speed for that entire component in which it is using.

In this thesis we are working at delay , power consumption and area for microcontroller designing . our results are coming better from previous work . The delay is coming 6.642ns (5.937ns logic, 0.705ns route) (89.4% logic, 10.6% route) for 16 bit microcontroller . here we are finding total LUT's 38 which is less from previous work .

Total power consumption is coming 0.088W which is very low according to previous paper .That paper is showing the results in Delay , power consumption , area but we have been decreased all the parameter by use pipelining concept .

Here we use clock for transfer the data parallel . We want transfer the parallel so we want a clock so that at which we can transfer the data . So we are using the clock at which we are sending the data parallel by pipeline .This is the reason that why our parameters are reducing. We have been shows all the graphs regarding this power consumption .

References

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