

Area Efficient Layout Design & Analysis of Full Subtractor

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ABSTRACT

The Main objective of this paper is to design Full Subtractor by using CMOS 65nm technology with less number of transistors and hence it is efficient in area and reduces the complexity. The design of Full subtractor has been obtained compared using auto generated layout, semi custom layout and fully custom layout. Performing the simulation comparison is made between three layouts between autogenerated, semicustom and fully custom on the basis of area. In this paper Fully custom layout is 45% area efficient than autogenerated and 41% than semicustom layout. Semi custom is 6% area efficient than autogenerated. Fully custom has better performance among the three layout techniques.

Keywords: Area, Full Custom, Full Subtractor, VLSI

I. INTRODUCTION

Combinational circuit is a type of digital circuit which is implemented by Boolean functions, where the output is a pure function of the present input only. The combinational circuit does not use any memory[1]. The previous state of input does not have any effect on the present state of the circuit. A combinational circuit can have an 'n' number of inputs and 'm' number of outputs[2]. For example adder, subtractor, multiplexer, demultiplexer, encoder, decoder etc. Full Subtractor is a combinational circuit which represents the smallest unit for subtraction in digital systems. It is not only used for arithmetic calculation in many device processors but also used in other part of processor for calculating address [3].

Arithmetic circuits are important part of Digital circuits. In the digital circuits, subtractor is one of the most critical components used in the processor of portable devices [4]. Hence the area and power efficient design of 1-bit Subtractor is necessary for design of small size portable devices. There are various possible logic styles that can give better performance as compared to the basic CMOS logic style. **Very-large-scale integration (VLSI)** is the process of creating an integrated circuit (IC) by combining thousands of transistors into a single chip. VLSI began in the 1970s when complex semiconductor and communication technologies were

being developed. The microprocessor is a VLSI device. Before the introduction of VLSI technology, most ICs had a limited set of functions they could perform[5]. ICs have three key advantages over digital circuits, size, speed and power consumption. To build an IC fabrication line, we must go one step further and design the layout. CMOS .A number of different IC fabrication technologies are available to us. The most important difference between technologies is the types of transistors they can produce[6]. CMOS can be designed by using Pmos and NMOS transistor and CMOS consumes no steady state power. Full subtractor is designed by using two half subtractors. For subtractors the basic building block is CMOS inverter. The performance estimation of full Subtractor is based on area .

II. SUBTRACTOR

Half Subtractor is a combination circuit with two inputs and two outputs (difference and borrow). It produces the difference between the two binary bits at the input and also produces a output (Borrow) to indicate if a 1 has been borrowed. In the subtraction (A-B), A is called as Minuend bit and B is called as Subtrahend bit.

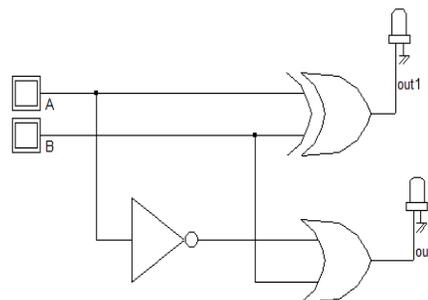


Fig.1. Logic diagram of Half subtractor

Here in this fig.1 half subtractor is shown. It produces two outputs out1 (difference) and out2 (borrow). A and B are two inputs. The Borrow output here specifies whether a '1' has been borrowed to perform the subtraction. The Half-Subtractor at the gate-level and truth table are shown in Fig 1 and Table 1.

Table 1: Half Subtractor Truth Table

A	B	Borrow(out2)	Difference(out1)
0	0	0	0
0	1	1	1
1	0	0	1
1	1	0	0

The Boolean expression for the two output variables are given by the equations

$$\text{Difference} = A \oplus B$$

$$\text{Borrow} = \bar{A}B$$

The full-subtractor is a combinational circuit which is used to perform subtraction of three bits. It has three inputs, A (minuend) and B (subtrahend) and C (subtrahend) and two outputs D (difference) and B (borrow) as shown in fig.2. The Truth table is as shown in Table 2.

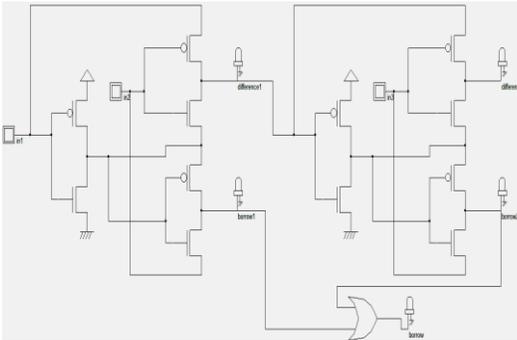


Fig.2. Logic diagram of Full subtractor

Table 2: Full Subtractor Truth Table

A	B	C	Diff.	Bout
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

The Boolean expression for the two output variables are given by the following equations

$$\text{Difference} = A \oplus B \oplus C$$

$$\text{Borrow} = A(\bar{B} \oplus C) + BC$$

III. LAYOUT DESIGN SIMULATION

In first method the schematic of full subtractor using two half subtractors is designed. Using Microwind software

the auto generated layout of full subtractor is created, and then simulate the layout. In this paper 65 nm foundry is selected. The figure 3 represents this autogenerated layout.

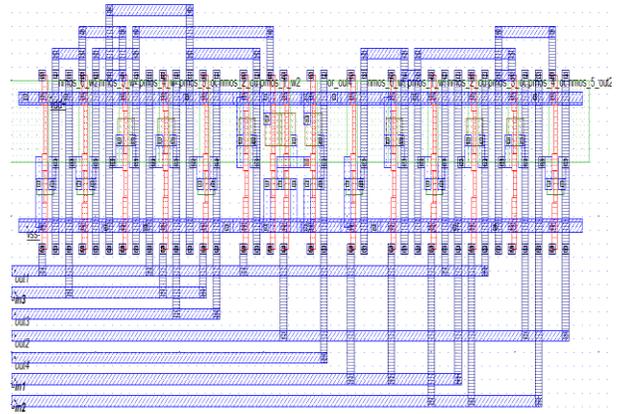


Fig. 3. Auto generated Full subtractor

This layout is checked for DRC if there is no error then it is simulated. And generated timing waveforms are verified on comparing to the circuit operation. The power is measured by the simulation result. The figure 4 shows the timing diagram of this automatic layout.

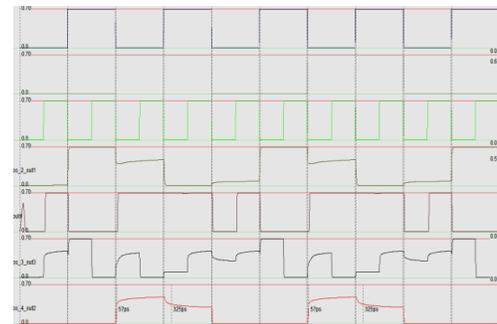


Fig.4. Timing Diagram of Automatic Generated Layout

We measure the power consuming by this layout and from the properties of layout area is measured. Here the consuming power is 1.76 μWatt . Area required for this particular layout is 117 μm^2 . Width is 16.4 μm and height is 7.2 μm . In second step we prepare layout using semicustom approach. In semicustom approach transistors are inbuilt. In this approach connections are made by the developer following lambda design rules. There is possibility of area reduction. Figure 5 represents the layout using semicustom approach.

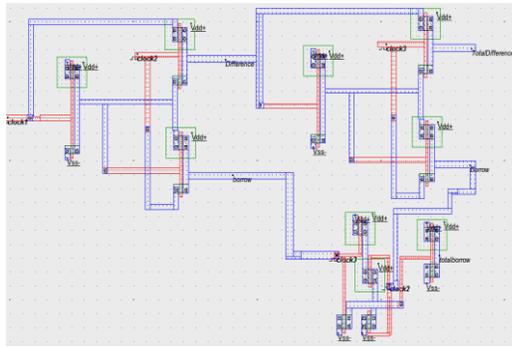


Fig. 5. Semi custom Layout of Full subtractor

The semicustom layout is checked for DRC if there is no error present in layout, the circuit is simulated and timing waveforms are generated. The generated timing waveforms are verified with the truth table or operation of original circuit. Figure 6 shows the timing diagram of semicustom layout.

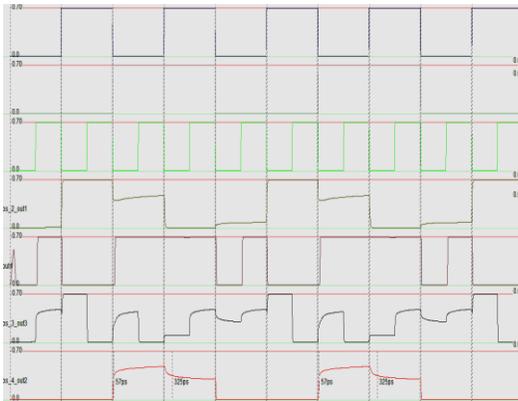


Fig.6. Timing Diagram of Semicustom layout

The power is observed from this particular simulation. Here power is 4.2 μ Watt, more than automatic layout. And area is calculated from the properties. Here the width is 13.3 μ m (381 lambda) and height is 8.3 μ m (236 lambda). In semicustom layout area is 96 μ m². In third step fully custom approach is used. **Full-custom** design is a methodology for designing integrated circuits by specifying the layout of each individual transistor and the interconnections between them. Full-custom design potentially maximizes the performance of the chip, and minimizes its area, but is extremely labor-intensive to implement. Measured width 7.7 (219- lambda) μ m and 8.6 μ m (245- lambda). Measured area is 65 μ m². But some amount of power is increased.

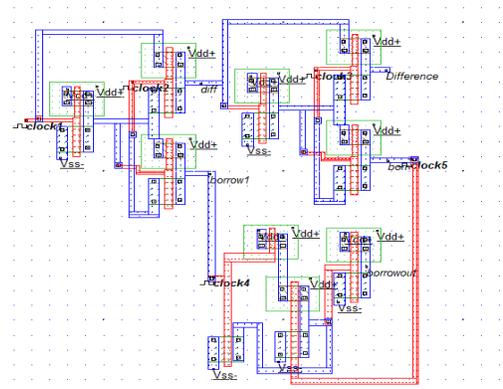


Fig.6. Full custom layout of Subtractor

Created layout is checked for DRC and simulate. The timing waveforms are verified with original circuit operation. Power is measured from this simulation . In full custom design approach there is high area reduction but some amount of power is incremented . In this layout power consumed is 8 μ Watt . Figure 7 shows the timing diagram of this fully customized circuit.



Fig.6. Timing Diagram of Semicustom layout

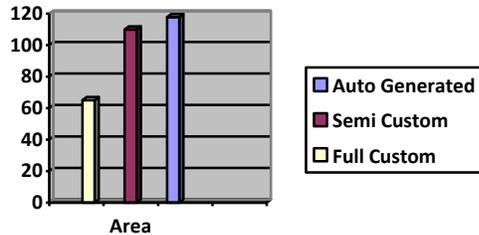
IV. RESULT COMPARISON

The performance of proposed full subtractor layout is compared with semicustom approach as well as automated layout. The performance parameters are Area and Power. From above results a comparative study can be done between three designing approaches. Table 3 shows comparative analysis.

Table 3: Comparative Analysis for Area and Power

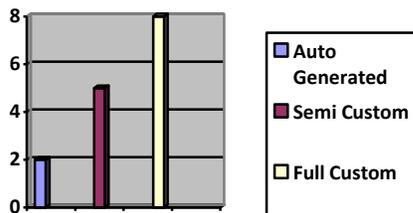
Parameters	Auto-Generated Layout	Semi-Custom Layout	Full-Custom Layout
Area(μ m) ²	117.8	110	65
Power(μ Watt)	2	5	8

Comparative analysis table shows that in terms of power the performance of automatic layout approach increases. In terms of area the full custom layout has better performance among three design approaches. Area graph of these three design approaches is shown below :



From the above graph we observed, there is a reduction of 45% in area with auto generated layout. And there is 41% reduction in area with semi custom layout. Performance is increases in terms of area required. This fully customized layout is used in compact size applications.

But more power is required in full custom approach . Comparative analysis in terms of power is done through the following graph.



From above graph it is observed that fully customized layouts consume more power among all semi customized and auto generated.

V. CONCLUSION

From the above result analysis it is clear that the fully customized layout is more efficient in terms of area. Fully customized layout is 45% is better than semi custom layout and 41% is better than auto generated layout approaches. So this design approach can be implemented where area reduction is the main consideration. In this approach power factor compensates for area.

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