International Journal of Scientific Research Engineering & Technology (IJSRET) ISSN: 2278–0882
EATHD-2015 Conference Proceeding, 14-15 March, 2015

Area Efficient CMOS Layout Design of Ring Counter

[1]Ankita Mahajan,[2] Rajesh Mehra
[1]ME Scholar & [2]Associate Professor
Department of Electronics & Communication Engineering
National Institute of Technical Teachers' Training & Research, Chandigarh, UT, India

ABSTRACT
In this paper a detailed area analysis of 2- bit ring counter is done. Ring counter is a sequential circuit and in this paper it is designed using a very low number of P-MOS and N- MOS. Area comparison has been done using three layout designs namely auto generated, semi custom and fully custom. As the chip size is reducing day- by- day area and power reduction become the first goal of the designers. So keeping this view in mind it is analyzed in this paper that CMOS layout design using full custom approach yields the good results. It has been analyzed that the area has reduced up to 43% in comparison to auto generated layout.

Key Words: 2- bit ring counter, Sequential circuit, C-MOS, P-MOS, N- MOS.

I. Introduction

According to Moore's Law transistors become faster, consume less power and are cheaper to manufacture. Even though an individual CMOS transistor uses very little energy each time it switches, the enormous numbers of transistors switching at very high rates of speed have made power consumption a major design consideration [1]. Power consumption of digital circuits is one of the critical parameter instigating many efforts in reducing the power dissipation of the logic blocks of digital system. Ring counter is one of the logic components which has several applications including control units, multiplier and divider architecture [2]. One of the important properties of a ring counter is that its output is one-hot encoded (i.e., there is always only a single '1 '-valued bit in its output and all other bits are zero). This property of the ring counter makes its output wide especially as the counter size increases [3].
In digital circuit theory, sequential logic is a type of logic circuit whose output depends not only on the present value of its input signals but on the past history of its inputs. Sequential logic is used to construct finite state machines, a basic building block in all digital circuitry, as well as memory circuits and other devices. Digital sequential logic circuits are divided into synchronous and asynchronous types. In synchronous sequential circuits, the state of the device changes only at discrete times in response to a clock signal. In asynchronous circuits the state of the device can change at any time in response to changing inputs. In a synchronous circuit, an electronic oscillator called a clock (or clock generator) generates a sequence of repetitive pulses called the clock signal which is distributed to all the memory elements in the circuit. The basic memory element in sequential logic is the flip-flop. The output of each flip-flop only changes when triggered by the clock pulse, so changes to the logic signals throughout the circuit all begin at the same time, at regular intervals, synchronized by the clock. The main advantage of synchronous logic is its simplicity. The logic gates which perform the operations on the data require a finite amount of time to respond to changes to their inputs. This is called propagation delay. The interval between clock pulses must be long enough so that all the logic gates have time to respond to the changes and their outputs "settle" to stable logic values, before the next clock pulse occurs. As long as this condition is met (ignoring certain other details) the circuit is guaranteed to be stable and reliable. This determines the maximum operating speed of a synchronous circuit.

II. Ring Counter

A ring counter is a type of counter composed of a type circular shift register. The output of the last shift register is fed to the input of the first register. There are two types of ring counters: (i) a straight ring counter or Overbeck counter connects the output of the last shift register to the first shift register input and circulates a single one (or zero) bit around the ring. For example, in a 4-register one-hot counter, with initial register values of 1000, the repeating pattern is: 1000, 0100, 0010, 0001, 1000... . Note that one of the registers must be pre-loaded with a 1 (or 0) in order to operate properly. (ii) A twisted ring counter, also called Johnson counter or Mobius counter (also Moebius), connects the complement of the output of the last shift register to the input of the first register and circulates a stream of one's followed by zeros around the ring. For example, in a 4-register counter, with initial register values of 0000, the

repeating pattern is: 0000, 1000, 1100, 1110, 1111, 0111, 0011, 0001, 0000... [4].

Ring counters are used in hardware logic design (e.g. ASIC & FPGA) to create complicated finite state machines. Ring counters are used to encode input pulses to decimal, octal and to other forms. Once a clock pulse is activated in these counters, only one of the FFs is "set", as just one bit "1" would rotate in the circuit [5]. An n- bit synchronous ring counter is built up by cascading n D flip- flops in a chain by synchronizing the flip- flops with the same clock and setting the first flip-flop to status '1'. Figure 1 shows an example of 4-bit ring counter.

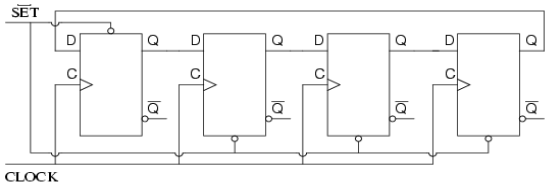

Figure 1. Four Bit Ring Counter

TABLE 1: 4-BIT RING COUNTER TRUTH TABLE

State	Q0	Q1	Q2	Q3
0	1	0	0	0
1	0	1	0	0
2	0	0	1	0
3	0	0	0	1
0	1	0	0	0
1	0	1	0	0
2	0	0	1	0
3	0	0	0	1
0	1	0	0	0

In this paper a 2- bit ring counter has been implemented using three different ways. This paper proposes the design of area efficient 2 bit- ring counter [6]. Further if the results are optimal then this 2-bit design can be implemented for higher bits ring counter. The three different methods are implemented using DSCH and Microwind software. The DSCH2 program is a logic editor and simulator. DSCH2 is used to validate the architecture of the logic circuit before the microelectronics design is started. DSCH2 provides a user friendly environment for hierarchical logic design, and simulation with delay analysis, which allows the design and validation of complex logic structures. The MICROWIND2 program allows designing and simulating an integrated circuit at physical description level. The package contains a library of common logic and analog ICs to view and simulate. MICROWIND2 includes all the commands for a mask editor as well as original tools never gathered before in a single module (2D and 3D process view, VERILOG compiler, tutorial on MOS devices). You can gain access to Circuit Simulation by pressing one single key. The electric extraction of your circuit is automatically performance and the analog simulator produces voltage and current curves immediately [7].

III. Layout Design Simulation

The first method is the designing of the ring counter in DSCH and generating its verilog file. Now in Microwind this verilog file is compiled and an auto generated layout is created. We can select different foundries available in the library of Microwind software. Here the selected foundry is 90 nm. Figure 2 represents this auto generated layout.

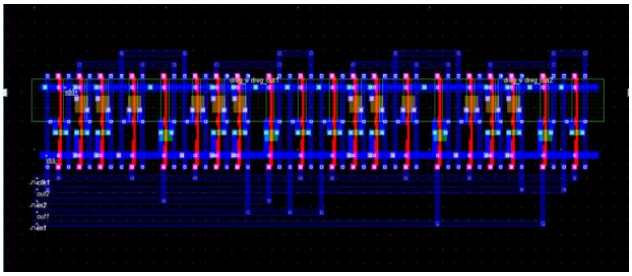

Figure 2. Auto Generated 2- bit Ring Counter

This layout is checked for DRC and if there is no error present in the layout then the layout is simulated. The output of the simulation is checked and if the output matches the output of the 2- bit ring counter then we further check the power and the area of this auto generated layout of 2- bit ring counter. Figure 3 shows the output of the 2- bit ring counter. Also power can be measured from the result of simulation.

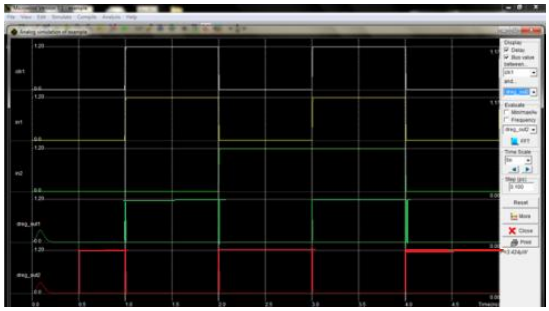

Figure 3. Output of Auto Generated 2- bit Ring Counter

The measured power here is 3.42µW. The area consumed here is 134.5µm^2.

Now the second step is to directly make use of in- built transistors the process being called as semi custom layout design. In this method the connections are made by the developer and hence there is a large possibility that area may get reduced. A D flip- flop is constructed using the semi custom layout of P- MOS and N- MOS [8]. Only five transistors were used to make the design of D type flip flop. Thus this design can be much more area efficient than the auto generated layout. Figure 4. represents the layout using the semi- customed transistors i.e. N- MOS and P- MOS.

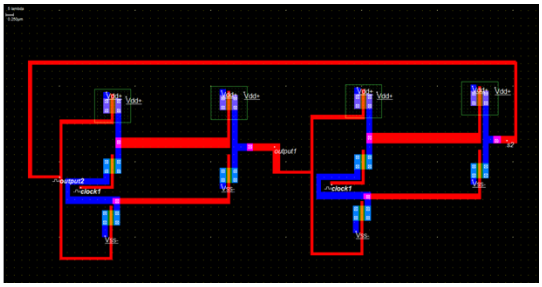

Figure 4. Semi Custom Layout of 2- Bit Ring Counter

When the layout is ready it is again checked for DRC and if there is no error present in the layout, the circuit is simulated and the outputs are obtained. The obtained output is verified with the truth table of 2- bit ring counter. If the truth table is verified we can further check the power and area consumed by this second method. Figure 5 shows the output obtained by simulating the above circuit.

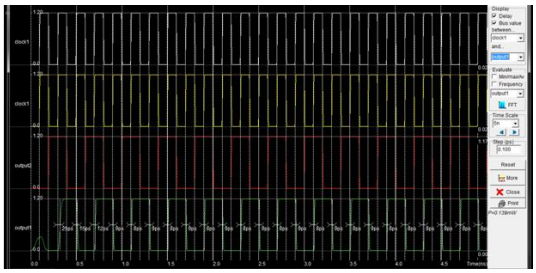

Figure 5. Output of 2- Bit Ring Counter using semi custom layout

Now check the results for power and area. Here the power consumed is 0.139 mW. The area consumed by this layout is 106.9 μm^2.

The third method is to create our own N- MOS and P- MOS transistors. Here the created transistors are called from the library and then connections are made. This new layout is shown by figure 6.

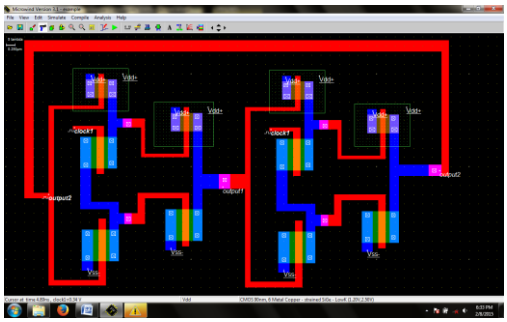

Figure 6. Fully Custom Layout of 2-Bit Ring Counter

Here the area measured is 76.1μm^2.

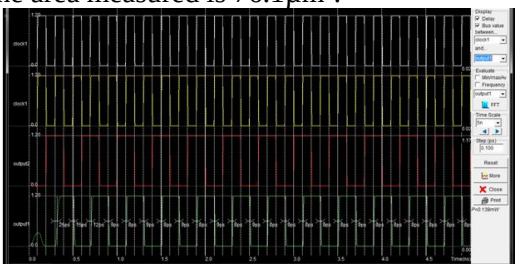

Figure 7. Output of 2- Bit Ring Counter using full custom layout

IV. Result Analysis

In this section, the area and power of different layout design has been compared using three different methods based on simulation results. A comparative analysis of table 2 shows that the power of fully custom layout design is more as compare to auto generated. But on the other side there is reduction of 43% in area. Also there is a slight reduction in power consumption from 0.139mW to 0.127mW in full custom layout design of ring counter. Tabular method chart have been used to compare the results

TABLE 2: Comparative analysis of Power and Area

Method	Power	Area
Auto Generated Layout	3.42µW	134.5µ m^2
Layout using in-built transistors	0.139 mW	106.9 μm^2
Layout using own created transistors	0.127m W	76.1 μm^2

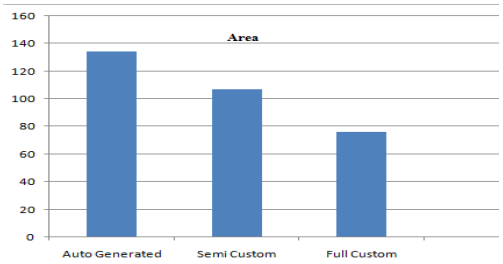

Figure7. Bar Chart Comparison of Area

V. Conclusion

From the above analysis it is clear that the layout with self created transistors is more efficient in terms of area. So this design can be implemented in the applications where area reduction is the main consideration. Here power factor can be compensated for area. A comparative analysis of this table shows that in terms of power, the layout generated using semi custom approach is increasing. But on the other hand in terms of area the auto generated layout is using more area in comparison to the layout using semi custom approach and the full custom approach. There is a reduction of 20% in area when auto generated layout is compared to layout using semi custom approach. When auto generated layout is compared to layout using full custom approach then there is a reduction of 43% in the area. Now when both the layout with semi custom and full custom approach is compared in terms of area then there is a reduction of 28% in the area.

Acknowledgement

The authors would also like to thank Director,
National Institute of Technical Teachers' Training & Research, Chandigarh, India for their constant inspirations and support throughout this research work.

References

[1] Neil H.E. Weste, David Harris, Ayan Banerjee, CMOS VLSI Design, Pearson Education Asia, Third Edition, pp. 4-5, 2009

[2] Cesar Albenes Zeferinol, Altamiro Amadeu Susinl, "SoCIN: a parametric and scalable network-on-chip," 16th Symposium on Integrated Circuits and Systems Design (SBCCI 2003), pp 169-174, Sept. 2003.

[3] Mohammad Dastjerdi- Mottaghi, Anahita Naghilou, Masoud Daneshtalab, Ali Afzali-Kusha, Zainalabedin Navabi, "Hot Block Ring Counter: A Low Power Synchronous Ring Counter," in IEEE, pp 58-62, 2006.

[4] B.R.B Jaswanth, R.V.S Rayudu, K.Mani babu, R.Himaja, L.Veda kumar, "A Design Of A Low Power Delay Buffer Using Ring Counter Addressing Schemes," International Journal of Technological Exploration and Learning, Vol. 2, Issue. 2, pp. 99-103, April 2013.

[5] Mehdi Askari, Maryam Taghizadeh, Khossro Fardad, "Design and Analysis of a Sequential Ring Counter for QCA Implementation," in Proc. Proceedings of the International Conference on Computer and Communication Engineering, Kuala Lumpur, Malaysia, pp. 933-936, May 2008.

[6] SURESH KUMAR.R, "Power and Area Efficient Design of Counter for Low Power VLSI System," International Journal of Computer Science and Mobile Computing, Vol. 2, Issue. 6, pp .435 – 443, June 2013.

[7] Upwinder Kaur, Rajesh Mehra, "Low Power CMOS Counter Using Clock Gated Flip-Flop," International Journal of Engineering and Advanced Technology, Vol. 2, Issue. 4, pp. 796-798, April 2013.

[8] Priyanka Sharma, Rajesh Mehra, "True Single Phase Clocking Flip-Flop Design using Multi Threshold CMOS Technique," International Journal of Computer Applications, Vol. 96, pp. 44-51, June 2014.

Authors

Ankita Mahajan received Bachelors of Technology degree in Electronics and Communication Engineering from Green Hills Engineering College, HPU, Shimla, India in 2009. She is pursuing Masters of engineering degree in Electronics and Communication Engineering from National Institute of Technical Teacher's Training and Research, Panjab University, Chandigarh, India. Her current research interests are in Very Large Scale Integration Design and Embedded System Design.

Rajesh Mehra received the Bachelors of Technology degree in Electronics and Communication Engineering from National Institute of Technology, Jalandhar, India in 1994, and the Masters of Engineering degree in Electronics and Communication Engineering from National Institute of TechnicalTeachers' Training & Research, Panjab Univsrsity, Chandigarh, India in 2008. He is pursuing Doctor of Philosophy degree in Electronics and Communication Engineering from National Institute of Technical Teachers' Training & Research, Panjab Univsrsity, Chandigarh, India. He is an Associate Professor with the Department of Electronics & Communication Engineering, National Institute of Technical Teachers' Training & Research, Ministry of Human Resource Development, Chandigarh, India. His current research and teaching interests are in Signal, and Communications Processing, Very Large Scale Integration Design. He has authored more than 175 research publications including more than 100 in Journals. Mr. Mehra is member of IEEE and ISTE.