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LAYOUT DESIGN SIMULATION OF AREA AND POWER EFFICIENT 10 TG FULL SUBTRACTOR

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Abstract
Full Subtractor is an essential component in designing various hardware circuits and variety of processors. Combinational logic has extensive applications in computing low power VLSI design. In the world of technology, it has become necessary to develop various new design methodologies with reduction in power consumption, area and number of transistors. In this paper, Full Subtractor has designed using 10-transistors on 32nm CMOS technologies. Three different layout design techniques has been used in this paper i.e.; auto generated, semi custom and fully custom layout design and comparison is done in terms of power and area. The fully custom full subtractor layout design has shown the improvement of 30.41%/74.21% in power dissipation and 13.19%/69.01% in area.

Key Words: *CMOS, Full Subtractor, Transmission gate (TG), XOR, XNOR, MUX, VLSI, and GDI.*

I. INTRODUCTION
In VLSI the increasing demand for low power can be addressed at various logic levels, such as circuit, and layout [1]. Power dissipation increases as the number of transistors increases on a single chip. The various industries have achieved a phenomenal growth over the last few decades, mainly due to the rapid growth in integration technologies (IC) and large scale systems design. The performance of the circuit is measured by the number of logic gates mounted on a monolithic chip. Subtractor is one of the most critical components of a processor, as it is used in arithmetic logic unit (ALU). The previous design of Subtractor consists 6T XOR-XNOR module which provide two intermediate signals which are provided to 2x1 MUX. These two signals act as two inputs signals and the third signal act as select line and difference of three inputs A, B and C act as output of 2x1 MUX. Second output Borrow is implemented by two AND gates and one OR gate. Previous 1-bit GDI Full Subtractor has been implemented using only 14 transistors i.e. difference has been obtained using 6T XOR-XNOR module and 2T 2x1 MUX and the Borrow is obtained by cascading the output of XOR-XNOR module with 6 more transistors [2]. CMOS logic families are used as low power logic as they are easy to design and the scaling of supply voltage allow the circuit to be used for wide performances in terms of speed. The transmission gate has the advantage of high speed and lower delay [3].

Subtractor is one of the most critical components used in the processor of various devices. In designing of small size portable devices subtarctor can be necessary [4]-[5]. Efficient Area and power consumption are the important issues in VLSI design which often conflict with the design methodology and act as barrier in designing of VLSI circuits. Many full subtractor designs have been proposed [4]. The transmission gate CMOS full subtractor uses transmission gate logic and realizes the complex function with a reduced number of CMOS transistors in comparison of CMOS full subtractor. The basic full subtractor has three inputs A (operand 1), Bin (operand 2) and C (operand 3) and two outputs which are difference and Bout (borrow). The logical expression for the outputs of full subtractor can be given by the following equations:

Difference = $A \oplus B_{in} \oplus C$ (1)

Bout = $\overline{A}\ B_{in} + B_{in}.C + C.\overline{A}$ (2)

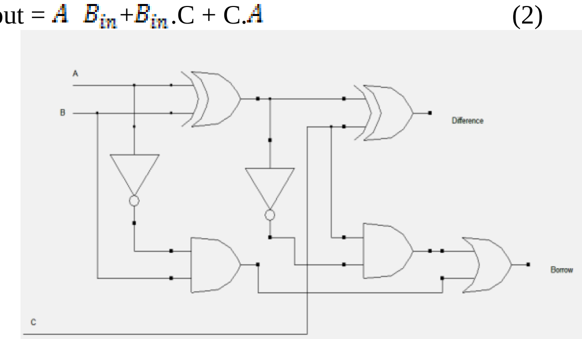

Figure1: Boolean circuit for Full Subtractor

The Exclusive-OR and Exclusive-NOR gates are commonly used components in designing of Full subtractor [5]. Full subtractor performance can be enhanced by improving the XOR/XNOR gates performance. The XOR/XNOR gates can be designed using logic gates i.e., AND, OR, and NOT. Efficient designing of these logic gates improve the performance of Full subtractor hence these gates are used as sub blocks in designing larger systems. Implementation of XOR/XNOR cell with minimum number of transistor is desirables as they are area efficient and power efficient in VLSI system [6]-[8].

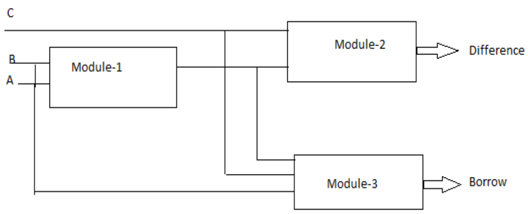

Figure2: Structure of Full Subtractor

Structured implementation of 1-bit Full subtractor using XOR/XNOR cell has been represented in figure2 [9]-[11]. Module-1 is represented as XOR/XNOR gate, which perform XOR or XNOR operation on inputs A and B. Module-2 is further represented as XOR/ XNOR gate, having inputs C and output of Module-1. The output of Module-2 is considered as Difference of full subtractor. Borrow logic could be given by Module-3 which works as a 2:1 multiplexer having inputs B, C and gives Bout as output [12].

II. FULL SUBTRACTOR SCHEMATIC DESIGN

A. XOR / XNOR cells and 2:1 MUX :

In this section the full subtractor cell design has been mentioned using XOR/XNOR gates and 2:1 multiplexer. Figure 3 and Figure 4 represents the schematics diagram of XOR and XNOR gates using 4-transistors respectively. DSCH schematic of 2:1 multiplexer which will be used to provide the borrow logic in full subtractor design has shown in Figure 5.

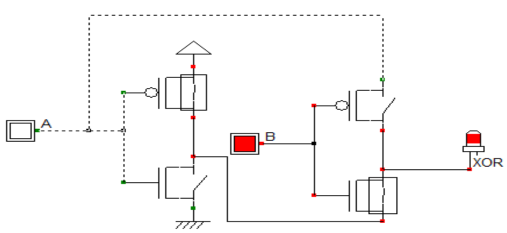

Figure 3: 4-Transistor XOR cell

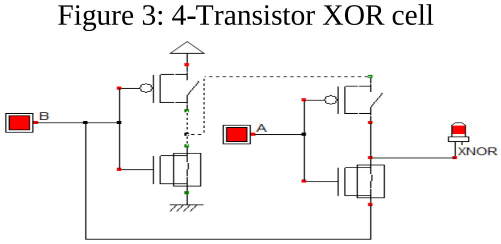

Figure 4: 4-Transistor XNOR cell

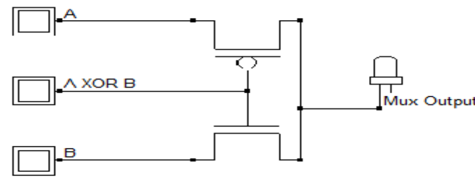

Figure 5: 2:1 Multiplexer

B. 10-Transistor Full subtractor schematic in DSCH:

Figure 6 and Figure 7 represent the Full subtractor schematic design in DSCH software using XOR and XNOR cells and 2:1 mux respectively.

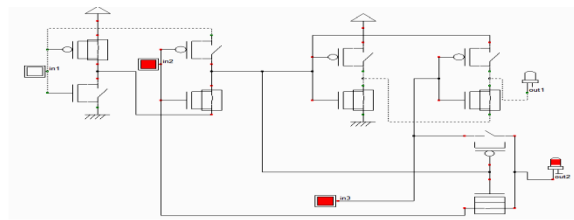

Figure 6: 10-TG XOR Full Subtractor

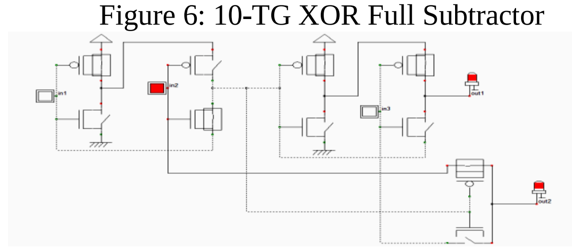

Figure 7: 10-TG XNOR Full Subtractor

III.LAYOUT DESIGN AND SIMULATION

In this paper two different approaches are adopted for layout designing. In first approach the auto generated layout has been obtained in µwind by compiling the verilog file generated by DSCH and the second approach through which
the layout is designed manually. The auto generated layout for XOR/ Full Subtractor and XNOR/Full Subtractor are shown in figure 8 and figure 9 respectively. Figure 10 and Figure 11 represent the semi custom layout for XOR/ Full Subtractor and XNOR/Full Subtractor respectively. Figure 12 and Figure 13 represent the fully custom designed layout for XOR/Full Subtractor and XNOR/Full subtarctor respectively.

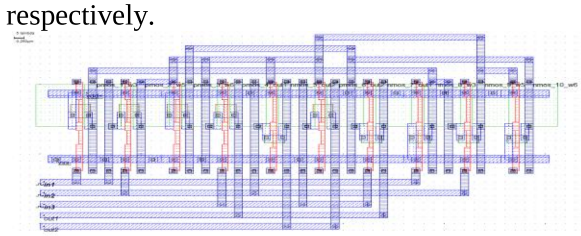

Figure 8: Auto generated Layout for XOR/FS

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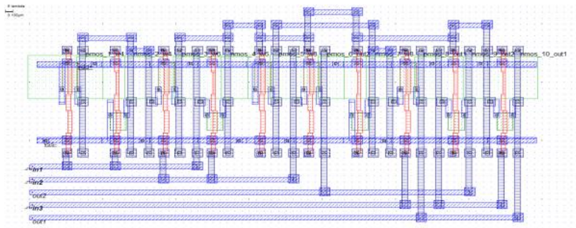
Figure 9: Auto generated Layout for XNOR/FS

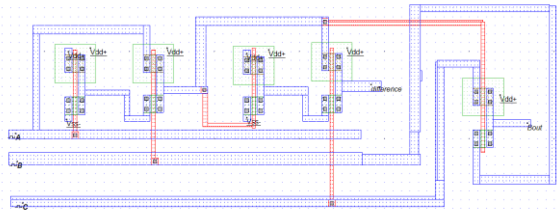
Figure 10: Semi custom de Layout for XOR/FS

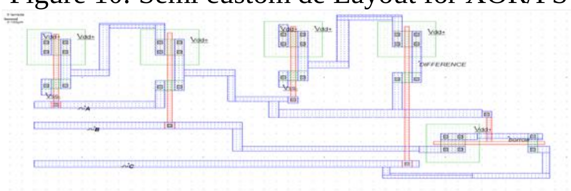
Figure 11: Semi custom designed Layout for XNOR/FS

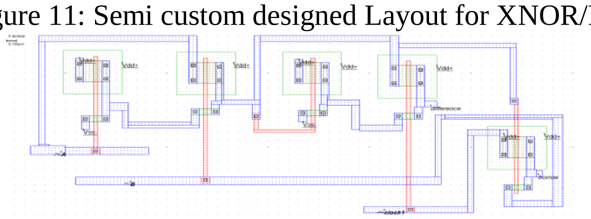
Figure 12: Fully Custom designed Layout for XOR/FS

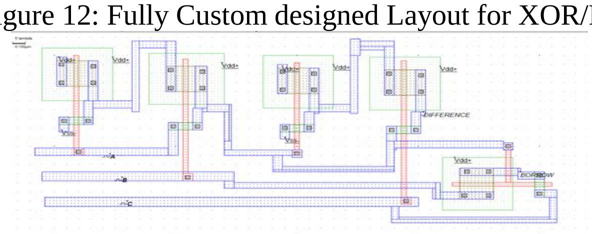
Figure 13: Fully Custom designed Layout for XNOR/FS

Figure 14, 15, 16, 17, 18 and 19 show the simulated results obtained from µwind for auto generated layouts, semi custom designed layouts and fully custom designed layouts for XOR/XNOR full subtractor circuit.

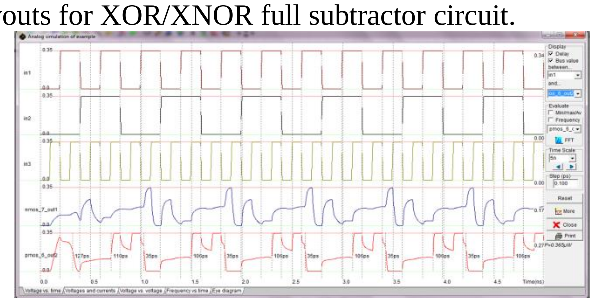
Figure 14: Analog simulation result for auto generated XOR/ FS.

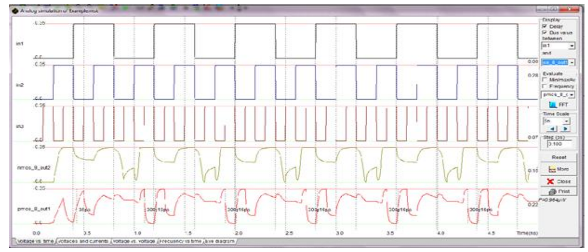
Figure 15: Analog simulation result for auto generated XNOR/FS.

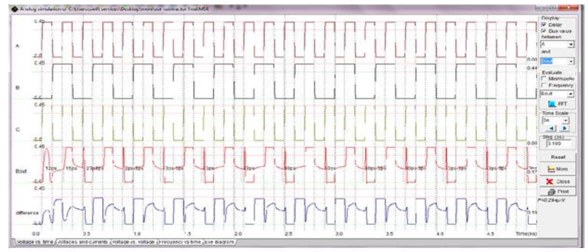
Figure 16: Analog simulation result for semi custom XOR/ FS

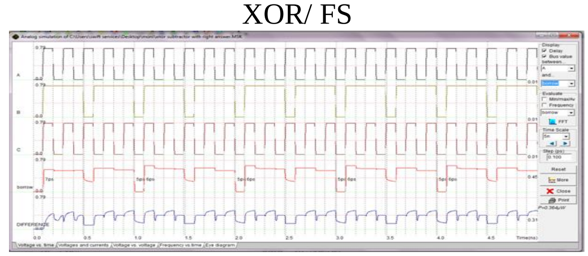
Figure 17: Analog simulation result for semi custom XNOR/FS

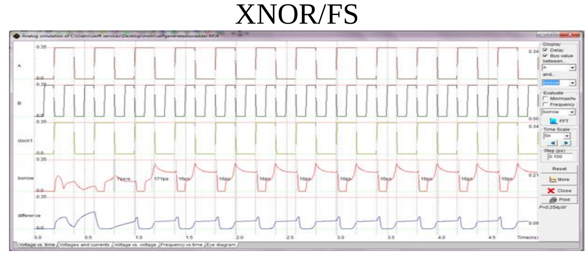
Figure 18: Analog simulation result for fully custom XOR/FS


Figure 19: Analog simulation result for fully custom XNOR/FS

IV. COMPARATIVE ANALYSIS

In this paper power and area consumption for the auto generated layout, semi custom designed layout and fully custom designed layout of XOR and XNOR based full subtractor has been compared. Table 1 shows the comparison of different powers. From table 1 it is clear that power consumption is less in fully custom designed layout as compared to auto generated and semi custom layout.

Table 1: Tabular comparison of Power consumption

Design	Power (microwatt)	
	XOR/FS	XNOR/FS
Auto generated layout	0.365 µW	0.764 µW
Semi custom designed layout	0.294µW	0.364 µW
Fully custom layout	0.254 µW	0.179 µW

Table 2 is represents the comparison of consumed area for different layout design approaches. From the tabular comparison it is clear that fully custom designed layout for XOR/XNOR Full Subtractor cell is area efficient than auto generated and semi custom designed layout.

Table 2: Tabular comparison of consumed area

Design	Area(in μm^2)	
	XOR/FS	XNOR/FS
Auto generated layout	14.4 μm^2	25.5 μm^2
Semi custom layout	13.2 μm^2	12.6 μm^2
Fully custom layout	12.5 μm^2	7.9 μm^2

Graphical comparison of consumed power and area for auto generated layout, semi custom layout and fully custom layout has been further shown by bar chart in Figure 20 and Figure 21 respectively.

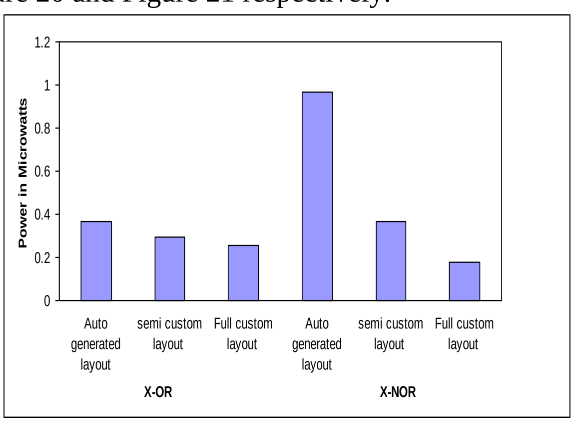

Figure 20: Graphical Comparison of Powers

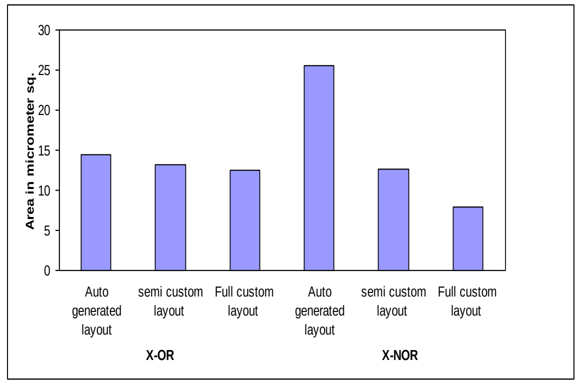

Figure 21: Graphical Comparison of Areas

V. CONCLUSION

In this paper Auto generation through DSCH, manual generation (semi custom and fully custom layout) using µwind layout are discussed and compared for XOR/XNOR full subtractor cell using 32 nm CMOS technology. These comparisons were made in terrns of power consumption and area. Simulated results show that manually generated layout has better power efficiency and less area consumption as compared to auto generated layout. It means fully custom layout show better performance in terms of power (range 30.41-13.6/ range 74.21-50.82) and area (range 13.19-5.30/ range 69.01- 37.30) when compared with auto generated layout and semi custom layout.

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