International Journal of Scientific Research Engineering & Technology (IJSRET) ISSN: 2278–0882
EATHD-2015 Conference Proceeding, 14-15 March, 2015

Layout design of D Flip Flop for Power and Area Reduction

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ABSTRACT
Design of low power device is now an essential field of research due to increase in demand of portable devices. In this paper a single edge triggered D flip flop with low power and low area requirements is proposed. This D flip flop has been implemented using 180 nm technology. The layout of D FF is designed using fully automatic, semi custom layout and fully custom layout techniques. It can be observed from simulation result the fully custom design has shown 38% reduction in area and 35% reduction in power as compared to fully automatic design. The overall design area is optimized to enhance the chip density. It can be used in various applications like digital VLSI clocking, buffers, registers, microprocessors etc.

Keywords: *D FF, NMOS, PMOS, SET-FF, VLSI*

I. INTRODUCTION

Power consumption is very important consideration in IC design. Two types of FF are found –single edge triggered (SET) and double edge triggered (DET). Single edge triggered is simple in design due to sampling data either on rising or on falling edge of clock , on the other hand double edge triggered sampled data on both clock edges. DET is energy efficient compared to SET. Double edge triggered Flip-flop provides poor performance due to more complex design [1]. There are also static and dynamic flip-flops. In dynamic FF if clock is removed, it produces faulty logic levels because of charge leakage from the capacitances of output node. In other way static FF keep output state even if there is no clock [2].
Many transistors had to be employed in the implementation of conventional FF and those FF required large area. Several efficient designs had been made. Still there is need of new design for further improvement of area and power consumption. In this paper a semi custom design has been suggested which is realized using few transistors and also occupy less area and consume less power than auto generated layout of design. [3-5].
There are so many FF configurations such as JK FF, T FF, D FF, in all above D FF is most simple and common. The D flip-flop is widely used. It is also known as a "data" or "delay" flip-flop. The D flip-flop captures the value of the D-input at a definite portion of the clock cycle (such as the rising edge of the clock). That captured value becomes the Q output. At other times, the output Q does not change.
Latches and flip-flops are the basic elements for storing information. One latch or flip-flop can store one bit of information [1-8].
The main difference between latches and flip-flops is that for latches, their outputs are constantly affected by their inputs as long as the enable signal is asserted. In other words, when they are enabled, their content changes immediately when their inputs change. Flip-flops, on the other hand, have their content change only either at the rising or falling edge of the enable signal. This enable signal is usually the controlling clock signal. After the rising or falling edge of the clock, the flip-flop content remains constant even if the input changes [1-10].
Latches are often called level-sensitive because their output follows their inputs as long as they are enabled. They are transparent during this entire time when the enable signal is asserted. There are situations when it is more useful to have the output change only at the rising or falling edge of the enable signal. This enable signal is usually the controlling clock signal. Thus, we can have all changes synchronized to the rising or falling edge of the clock. An edge-triggered flip-flop achieves this by combining in series a pair of latches [11-13]

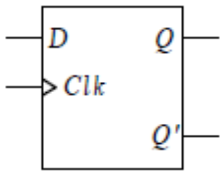

Figure 1: D Flip flop Symbol

Q	QNEXT	D
0	0	0
0	1	1
1	0	0
1	1	1

Figure 2: D Flip flop Excitation table

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II. D FLIP FLOP DESIGNS

The D-latch has many applications in digital circuit design, primarily for temporary storage of data or as a delay element. The circuit shown in Figure 3 shows a basic two-inverter loop and two CMOS transmission gate (TG) switches. The TG at the input is activated by the clock signal, whereas the TG in the inverter loop is activated by the inverse of the clock signal. Thus, the input signal is accepted (latched) into the circuit when the clock is high, and this information is preserved as the state of the inverter loop when the clock is low [6]

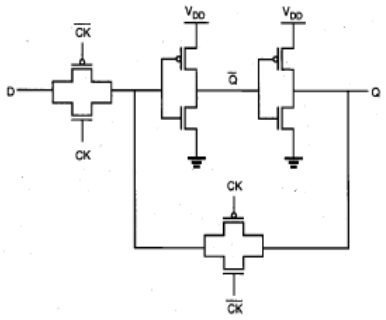

Figure 3: D Flip flop using transmission gate

The circuit shown in figure 4, shows CMOS implementation of D FF using 10 transisstor. The circuit consist of two tristate inverters and driven by clock signal and inverse of it. If clock becomes high, the first tri state inverter behaves as the input switch with the input signal.On the other hand second tristate inverter shows high input impedance state and output is following the input signal. If the clock signal becomes low , second trisate inverter completes the two inverter loop which hold its state until the next clock signal [6].

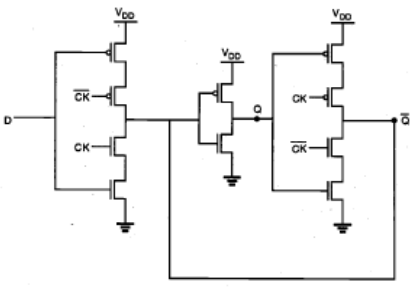

Figure 4: D Flip flop using tri state

Figure 5 Shows positive edge triggered 5 Transistor D latch. If Clock and input IN becomes high then the transistors M1, M5 shows off condition and remaining transistors M2, M3, M4 shows on. The output becomes high. During on clock period whatever is the value of input it becomes output.

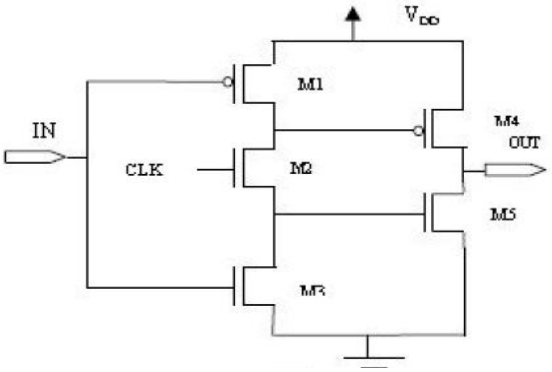

Figure 5: D Flip flop using 5 transistors

Minimum power consumption is necessary for high performance VLSI systems. In digital CMOS circuit there are three sources of power dissipation, the first occurs due to signal transition, the second is from short circuit current which flows directly from supply to ground terminal and the last comes due to leakage currents. As technology scales down the short circuit power becomes comparable to dynamic power dissipation [5-6].

III. PROPOSED LAYOUT

This paper aims the modification of the 5-transistor design to reduce the overall area and power consumption such that the design becomes better applicable for the low power applications. To continue with this, the design is first modified by creating the semi custom layout of design with pre defined transistors layout on Microwind platform. Figure 6, shows fully custom layout design of flip flop. In this design layout of all NMOS and PMOS are own created. Then connections are made with metal and poly silicon.

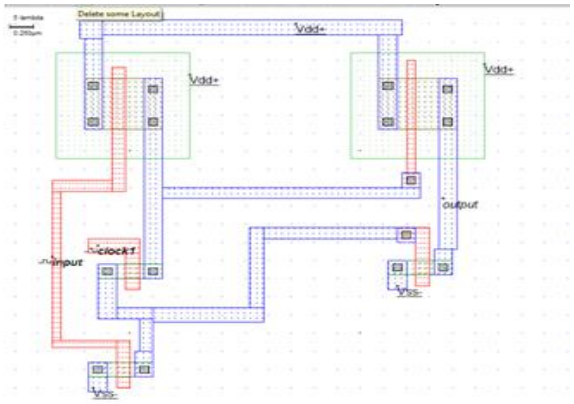

Figure 6. Proposed fully custom lay out of D Flip flop

IV. SIMULATION AND RESULTS

The designs are implemented using Microwind tool version 3.1.The circuits are simulated using 180 nm meter technology. The waveform of the proposed SET D FF is shown in figure 7. Using same technology, the designs from references [5], [6] were also simulated.

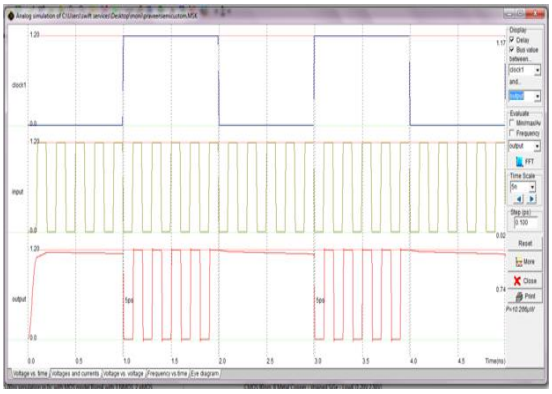

Figure 7: Proposed D Flip flop layout waveforms

Figure 8 shows schematic of D FF shown in figure 2. Design used 10 no. of transistors. It has two clock signals, one is positive and other is negative. If clock becomes high , LED Q output is similar to input switch.Q_MP is complement of Q. The design is implemented using DSCH sotware.

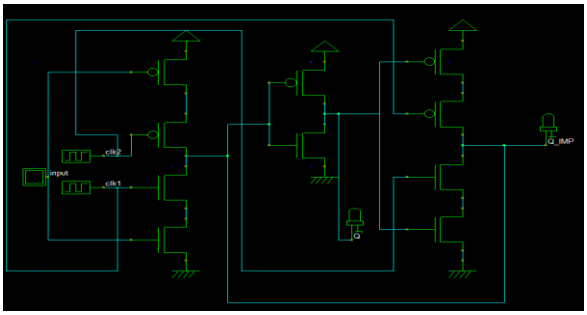

Figure 8: Schematic of D Flip flop

Figure 9 shows schematic of D FF shown in figure 3. Design used 5 no. of transistors. It has one clock signal. If Clock and input becomes high, The LED out 1 becomes high. The design is implemented using DSCH sotware to calculate area and power consumption.

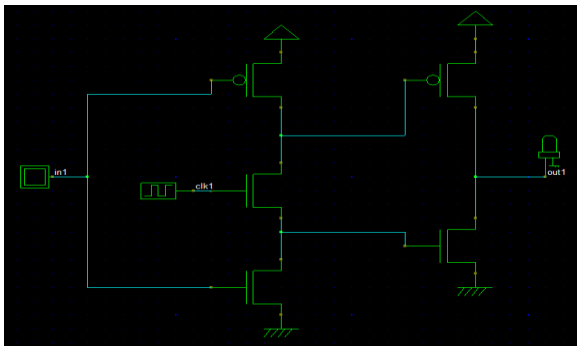

Figure 9: Schematic of D Flip flop

Figure 10 shows auto generated layout of D FF shown in figure 9 using Microwind tool with 180 nm technology.

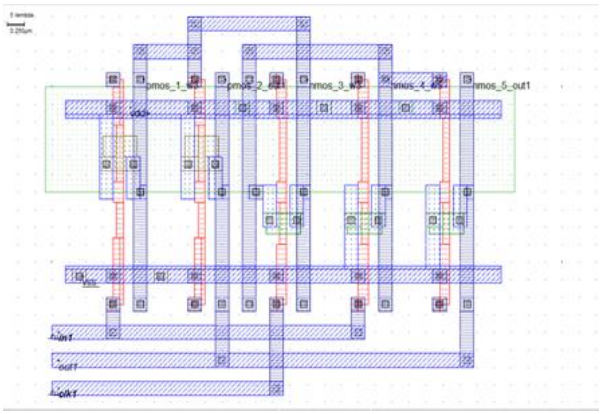

Figure 10: Auto generated layout of D Flip flop

Figure 11 shows semi custom layout of D FF shown in figure 9 using Microwind tool with 180 nm technology. In this design layout of all NMOS and PMOS are called from library.

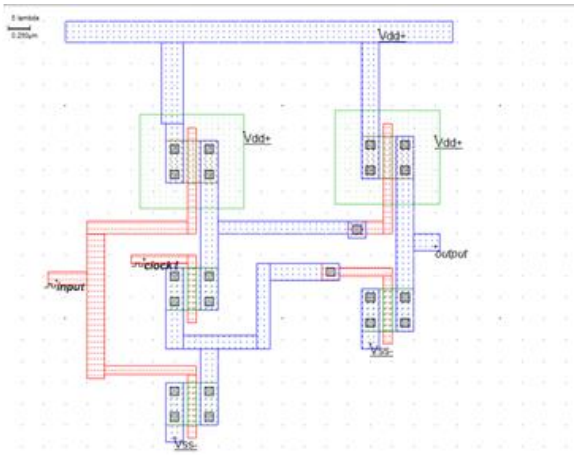

Figure 11: semi custom layout of D Flip flop

The functionality of the proposed layout has been verified as show in table I and a comprehensive study of power dissipation has been done with different Designs.
From the table I it is obvious that the power consumption decreases from auto generated layout design to proposed fully custom layout design.

Table I. Power / Area Consumption Between different SETDFF configuration and proposed layout

S.NO.	Auto Generated		Semi Custom	Fully custo m
	With 10 transist or	With 5 transist or	With 5 transistor	
Average Power (µW)	20.037	15.493	10.286	9.976
Average Area (µ m^2)	80.0	37.2	24	23

The functionality of the proposed layout has been verified in terms of area as shown in table I and a comprehensive study of area has been done with auto generated Designs.
From the table I it is obvious that the area consumption decreases from auto generated layout to proposed fully custom layout design.
It can be easily observed that there is considerable improvement in power consumption (as shown in table I) and area (as shown in table I) from auto generated design to fully custom design.

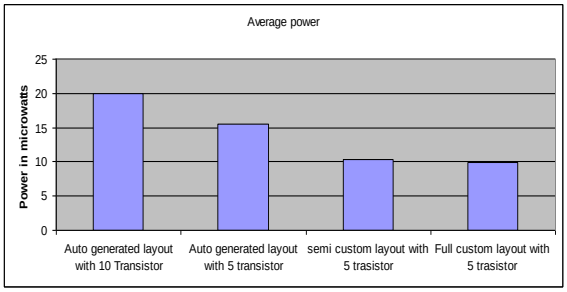

Figure 12: Graphical comparison of average power

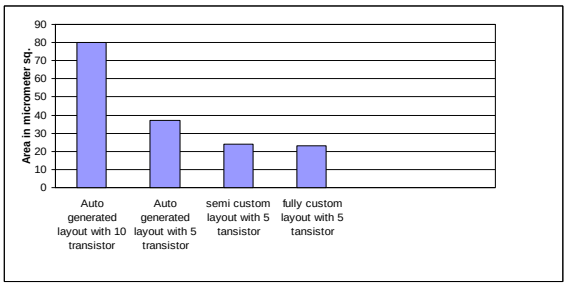

Figure 13: Graphical comparison of average area

V. CONCLUSION

In this paper, the D flip flop is implemented using various no. of transistors. In low power applications, area and power consumption by the device are the main technological aspects to prefer a design over the other designs. The fully custom design of SET D flip-flop shows better performance in terms of power dissipation and area among designs discussed in present article. The relative percentage power reduction in the proposed design is from 35 % to 50 % with respect to the previous designs. Design also has reduction in area from 38 % to 71.1 %

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