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Area and Power Efficient CMOS De-multiplexer Layout on 90nm Technology

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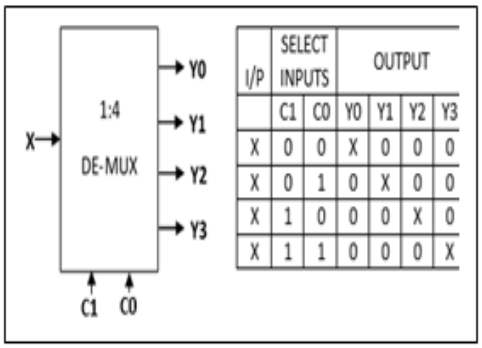
Abstract
Power dissipation in low powered devices is one of the most important considerations now days. It is very evident that hand held devices such as smart phones, calculators, tablets and laptops etc., which run on battery power, consume very low power for calculations and other operations. In this paper de-multiplexer has been designed using CMOS. In this paper the de-multiplexer has been designed with the help of 36 transistors using 90 nm CMOS technology. Two different layout design techniques have been discussed in this paper i.e.; auto generation technique and semi custom layout design. Designed layouts are compared in terms of power and area consumption. The semi customized de-multiplexer layout has shown the improvement of in power consumption and in area.

Key words— *De-multiplexer, CMOS, NMOS, Power dissipation, Combination logic, AND, NOT*

I. INTRODUCTION
Multiplexers and de-multiplexers are common building blocks of data paths and are used extensively in numerous applications including processor buses, network switches and digital signal processing stages incorporating resource sharing. The reduction of the power consumption by any VLSI circuit basically depends on the some parameters viz. reducing the number of transistor, reducing the size of the transistor, input re-ordering, reducing the capacitance etc. It is generally believed that low power designs need to have minimum transistor size. Most of the low-power design techniques are effective only for specific types of circuits and applications. Delay and power dissipation of a circuit have also emerged as major concerns of designers and depend on the number of transistors used in the circuit. When the number of transistors is more the capacitance is more due to which the delay is more [1-4] so here our aim is to reduce the delay and power dissipation. In this paper the author is applying technique like reducing the number of transistors, switching off some part of circuit during different input conditions and using different elements in the implementation of the circuit to reduce the overall power consumption. The rest of the paper is organized as follows: The section II explains the working of a de-multiplexer circuit, the section III explains the two circuits of de-multiplexer one made using AND gates and another made using CMOS and their timing diagram, section IV shows the layout diagram of two circuits with their analog simulation results provides comparison result between two designs. Finally the paper is concluded in section

II. DE-MULTIPLEXER
Digital computers process and transfer tremendous amount of digital signal. It would be prohibitive to make separate straight wire connections for the transfer of all this data within the computer with the procedure of multiplexing, a single wire is used to transfer data from multiple sources from the sending end. Now at the receiving end this data from various sources needs to be segregated for distribution to intended recipients. The device catering this need is a de-multiplexer. [5-10]. the graphical symbol and truth table of a de-multiplexer circuit is shown in Fig. In the circuit C1 and C0 are selection bits and X is the data bit. Depending upon the states of the selection bits, the data X is transferred to one of the four output connections. The routing of data bit on different output connections based on states of the selection bits is shown in Fig. 1.



I/P	SELECT INPUTS		OUTPUT			
	C1	C0	Y0	Y1	Y2	Y3
X	0	0	X	0	0	0
X	0	1	0	X	0	0
X	1	0	0	0	X	0
X	1	1	0	0	0	X

Fig. 1 Demultiplexer and its truth table

III. DE-MUX DESIGN SIMULATION
Conventional de-multiplexer circuits are made using AND gates and inverters (NOT gates). In order to design

a 1x4 de-multiplexer circuit, two inverters and four numbers of three input AND gates are required .A single AND gate with three inputs requires eight MOS transistors to be used for implementation. In this way the number of transistors used for implementing total four numbers of three input AND gates becomes thirty two.
In addition to this, the number of transistors required to implement two inverters are four. In all the implementation of 1x4 De multiplexer using the conventional method requires thirty six transistors. The implementation of conventional de-multiplexer circuit using AND gates and inverters are shown in Fig. (2).

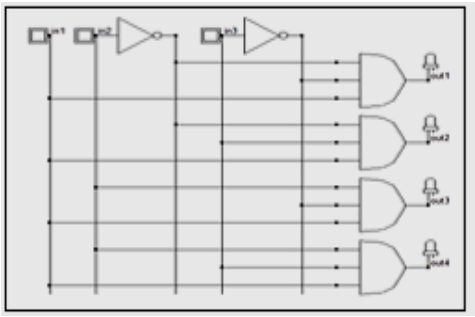


Fig 2. Conventional De-multiplexer

The De-multiplexer circuit shown in above figure works in the following manner: For the time when the input IN2 and IN3 are low, the first AND gate output will be high and the input will be redirected to the OUT1 LED. When IN1 and IN2 are 0 and 1 respectively, the input is directed to OUT2 LED. Next condition is when the IN1 and IN2 are 1 and 0 respectively, in this condition the third AND gate from top becomes active and input is directed to OUT3 LED. Last condition is when IN1 and IN2 both are 1, in this condition, the last AND gate from top becomes active and input is directed to OUT4 LED. The timing diagram of the de-multiplexer is shown in Fig. 3

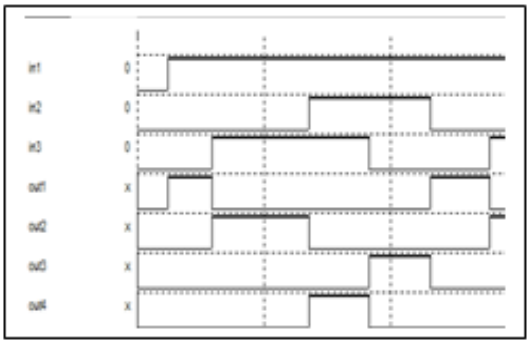


Fig 3. Timing diagram of 1x4 de-multiplexer

In this design of De-multiplexer 18 numbers of PMOS and as well as NMOS transistors, such way total 36 CMOS transistors are needed. This reduction in the number of transistor helps in reduction of the power consumption of the circuit that can be done using transmission gate. The new De-multiplexer circuit shown in Fig 4 works similar to the conventional de-multiplexer. Based on the select bits state i.e. 00, 01, 10 and 11, the input is directed to outputs OUT1, OUT2, OUT3 and OUT4 respectively. The timing diagram of the de-multiplexer is shown in Fig 5.

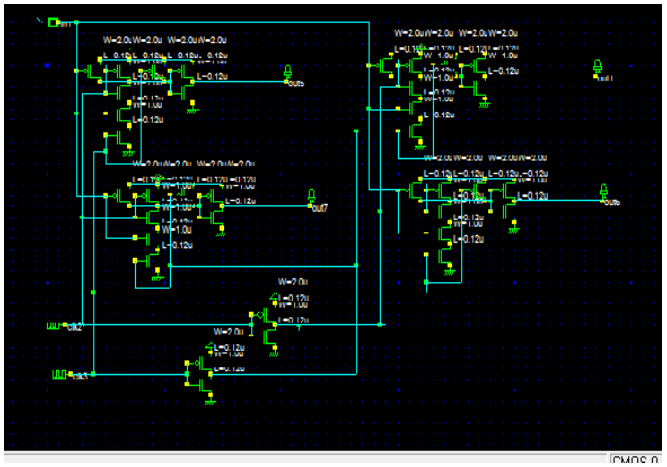


Fig 4. De-multiplexer using CMOS transistors

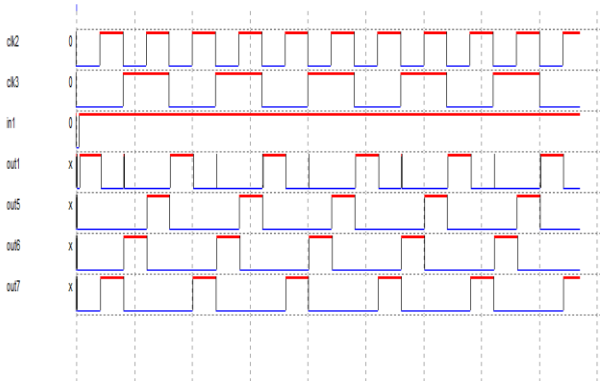


Fig 5 Timing diagram of 1x4 Demux using CMOS

IV. LAYOUT RESULT AND DISCUSSION

The main area of analysis in this paper is power consumption using auto generated and proposed lay out circuit and also compare the area of each lay out. The de-multiplexer circuit is design using DSCH and auto generation is done using MICROWIND. The auto generated layout is as shown in the Fig. 6. The auto generated wave form the De-multiplexer circuit currents using CMOS is as shown in the figure 7.

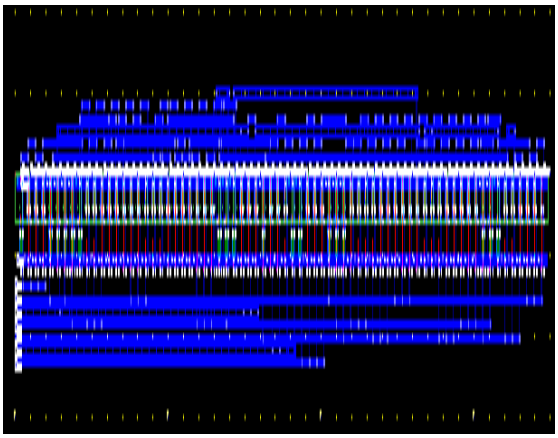


Fig 6 Auto generated layout of De-multiplexer

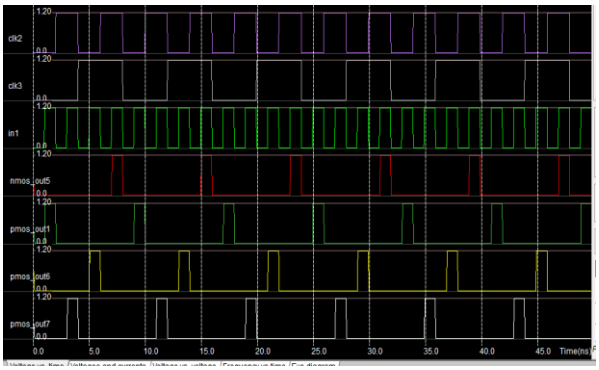


Fig7 auto generated timing diagram of de multiplexer

In the auto generation the power will be 40.024 µW .the generated area 750.83µm^2 (having the width 87.3µm and the length of the lay out will be 8.6µm). The proposed layout is generated in MICROWIND and simulated. The area of the created layout will be 416.8 µm^2 (having width 13.8 µm and length 30.2 µm.

The power will be 142 µW. The Fig 8 shows the proposed layout of the 1x4 De-multiplexer and Fig 9 shows the corresponding output of the De-multiplexer using proposed layout generated by the software.

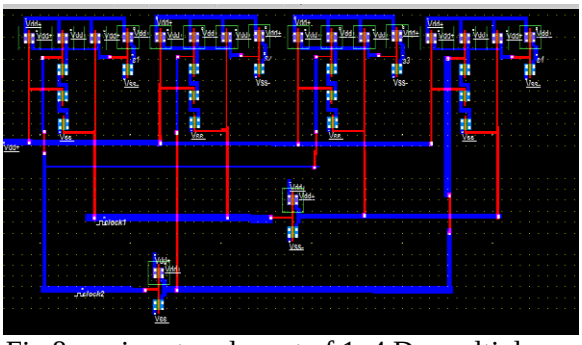


Fig 8 semi custom layout of 1x4 De-multiplexer

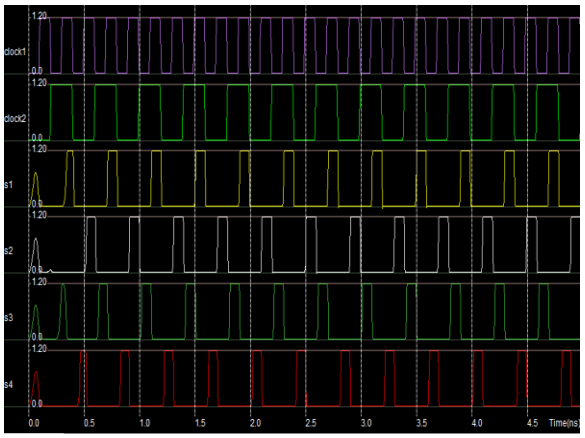


Fig 9 semi custom timing diagram of de multiplexer

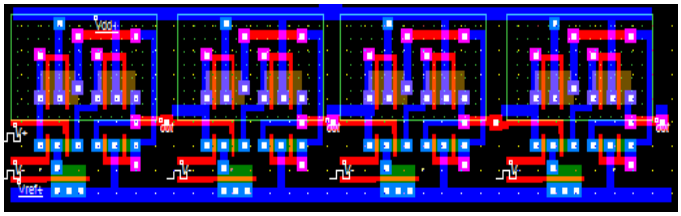


Fig 10 full custom timing diagram of de multiplexer

V. COMPARATIVE ANALYSIS

In this paper power and area consumption for the auto generated layout and manually generated layout of CMOS based 1x4 De-multiplexer has been compared. Table 1 is showing the comparison of power and area of auto generated lay out and semi custom generated lay out. From table 1 is clear that power consumption is less in manually designed layout as compared to auto generated layout. From the tabular comparison it is clear that manually designed layout for 1x4 De-multiplexer is area efficient than auto generated layout from DSCH.

Table 1: Tabular comparison of Power consumption

Design	Power (in µwatt)	Area (in µm^2)
Auto generated layout	142 µW	750.8 µm^2
Semi custom layout	40.024µW	416’8 µW
Full custom layout	202 µW	982.9 µW

VI. CONCLUSION

In this paper two different approaches for layout designing: Auto generation through DSCH and semi custom layout designing using µwind are discussed and compared for 1x4 De multiplexer using 90 nm CMOS technology. These comparisons were made interns of power and area. Simulated results in this paper show that semi customized design has better power efficiency and consumes less area as compared to auto generated layout. It means self generated layout always show better performance in terms of power and area as compared to auto generated layout .

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