CMOS 4-bit Multiplier design & simulation using different foundry

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ABSTRACT

Every time there is a requirement for a fast and energy-efficient multiplier in electronics industry especially digital signal processing (DSP), image processing and arithmetic units in microprocessors. Multiplier is such an important element which contributes substantially to the total power consumption of the system. Multipliers of various bit-widths are frequently required in VLSI from processors to application specific integrated circuits (ASICs). In this paper, proposed 4-bit multiplier has been taken which is then analyzed and comparison has been done on account of the power and surface area. The simulations in 45nm, 65nm and 90 nm CMOS technologies were done. The multipliers using 45 nm CMOS technology is better in terms of power and surface area as compare to 65 nm and 90 nm COMS technologies.

KEYWORDS: CMOS, VLSI, Multiplier, Power consumption, CMOS technology.

1. INTRODUCTION

The multiplier is one of the key hardware blocks in most of the digital and high performance systems such as digital signal processors and microprocessors. Multiplication consists of three steps: partial product generation (PPG), partial product reduction (PPR) and finally carry propagate addition (CPA). Different multiplication algorithms vary in the approaches of PPG, PPR and CPA [1].

Multiplication is one of the arithmetic operations performed by multiplier in the various analog and digital circuits. The speed and power dissipation are the important parameters which should be taken into consideration in digital circuits. In order to achieve energy efficient and low power VLSI (Very Large Scale Integration) circuits, different multiplication algorithm will be used to illustrate methods of designing different cells. Binary multiplication can be achieved by several approaches. A combinational circuits of tree multiplier, with a one-sided reduction tree and a ripple-carry adder as the final stage is called an array multiplier. More number of additions can be performed by chained with previous output but it has worst case delay. Hence speed is reduced. Then, the fastest Wallace tree multiplier has been introduced for minimum propagation delay. However, the Wallace multiplier has complex layout [2].

Multiplier circuits represent intensively used blocks in analog signal processing structures. The motivation for designing these computational structures is related to their extremely wide range of applications in analog signal processing, such as adaptive equalization, frequency translation, waveform generation and curve-fitting generators, amplitude modulation, automatic gain control, squaring and square rooting, rms-dc conversion, neural networks, and VLSI adaptive filters, or measurement equipment. Based on sub-threshold operated MOS transistors, the realization of multiplier/dividers requires simple architectures. In order to improve the frequency response of the computational structures and to increase their -3 dB bandwidth, many analog signal processing functions can be achieved by exploiting the squaring characteristic of MOS transistors biased in saturation. In multiplier structures were presented with single-ended input voltages, the linearization of their characteristics being obtained using proper squaring relations between the input potentials [3].

2. MULTIPLIER ARCHITECTURES

The wide-bit addition is vital in many applications such as ALUs, multiply-and accumulates (MAC) units in DSPs, and , versatile microprocessor. It is also important for the performance of direct digital frequency synthesizers (DDFSs) where it is used as a phase accumulator. Numerous multiplier implementations exist whereas some are good for low power dissipation and some takes least propagation delay [4]. In multiplication, multiplicand is added to itself a number of times as specified by the multiplier to generate product. In this section, two different 4-bit multiplier architectures are designed.

2.1 ARRAY MULTIPLIER

In array multiplier the two basic functions, partial product generation and summations are combined. For unsigned $N \times N$ multiplication, $N2+N-1$ cells (where $N2$ contain an AND gate for partial product generation, a full adder for summing and $N-1$ cells containing a full adder) are connected to produce a multiplier. This array generates N lower product bits directly and uses a carry-propagate adder, in this case a ripple carry adder, to form the upper N bits of the product [3].
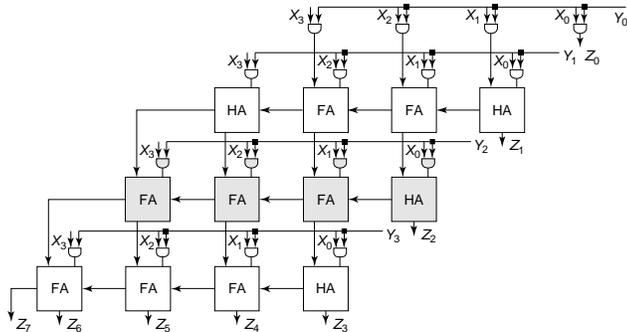

Figure 1: Array multiplier design flow

2.2 WALLACE TREE MULTIPLIER

C.S Wallace has suggested the fastest multiplier in 1964. Wallace is a tree of CSA designed for minimum propagation delay. It is implemented by adders using parallel multiplication resulting in less delay. Carry save adder method is used in order to reduce the number of stages. Wallace tree sums up same weight of three bits and produces output which is said to be compressors [4].

The Wallace tree multiplier is considerably faster than a simple array multiplier because of its non linearity. However in addition to the large number of adders required the Wallace trees wiring is less regular and more complicated. As a result, Wallace trees are often avoided by designers, while design complexity is concerned. The Wallace tree multiplier is a high speed multiplier. The summing of the partial product bits in parallel using a tree of carry save adders became generally known as the "Wallace Tree". Three step processes are used to multiply the numbers.
 Formation of bit products.
 Reduction of the bit product matrix into a two row matrix by means of a carry save adder.
 Summation of remaining two rows using a faster ripple carry adder.

In the Wallace tree method, three single bit signals are passed to a one bit full adder which is called a three input Wallace Tree circuit, and the output signal (sum) is supplied to the next stage full adder of the same bit, and the carry output signal is therefore passed to the next stage full adder located at a one bit higher position [5].
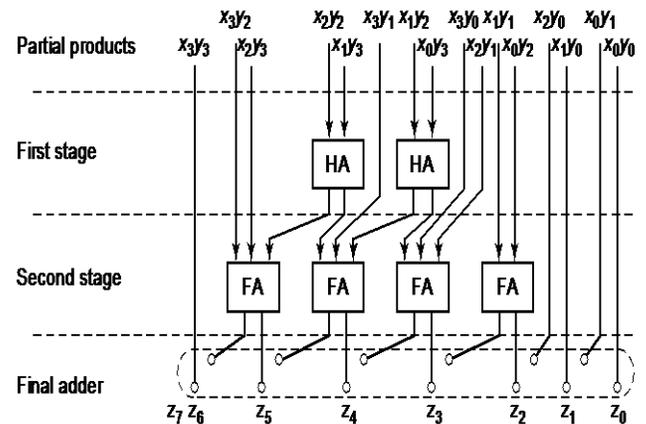

Figure 2: Wallace tree multiplier design flow

A. Characteristics of Multipliers

There are three main components of power consumption in digital CMOS VLSI circuits.

1. *Switching Power:* consumed in charging and discharging of the circuit capacitances during transistor switching.

2. *Short-Circuit Power*: consumed due to short-circuit current flowing from power supply to ground during transistor switching. This power more dominates in Deep Sub Micron (DSM) technology.

3. *Static Power*: consumed due to static and leakage currents flowing while the circuit is in a stable state. The first two components are referred to as dynamic power, since power is consumed dynamically while the circuit is changing states. Dynamic power accounts for the majority of the total power consumption in digital CMOS VLSI circuits at micron technology [6].

$$P_{avg} = P_{dynamic} + P_{static}$$
$$= (P_{Switching}+P_{Short\text{-}Circuit})+P_{Leakage}$$

B. Applications of Multiplier

The potential usages of proposed design are –

* High Speed Signal Processing that includes DSP
   based applications.

- • ☐ DWT and DCT transforms used for image and Wide signal processing.
- • FIR and IIR Filters for high speed, low power filtering applications.
- • ☐ Multirate signal processing applications such as digital down converters and up converters.

3. SIMULATION AND RESULTS

The 4-bit multipliers are compared based on the performance parameters like surface area and power dissipation. To achieve better performance, the circuits are designed using CMOS process by Microwind 3.1 in 45nm, 65nm and 90 nm technology. The proposed 4-bit multiplier circuit shown in figure 3, uses two 2-bit X-OR and six 2-bit AND logic gates.
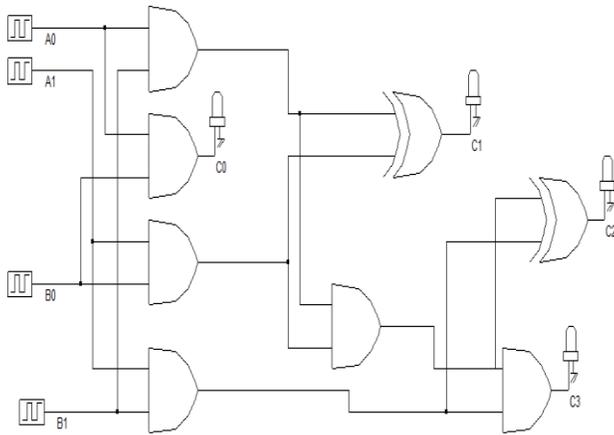

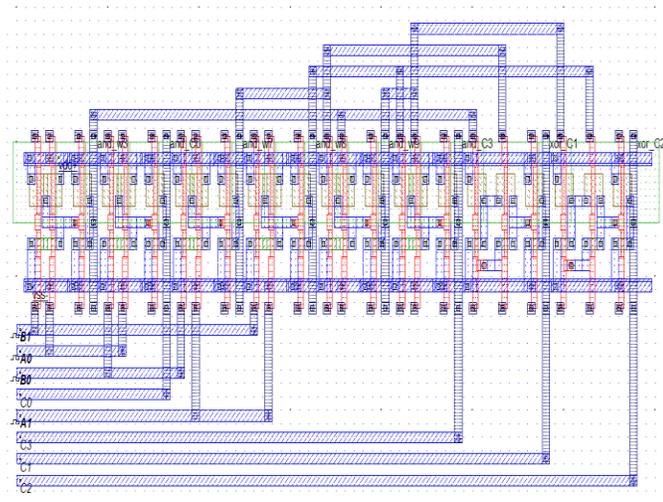Figure 3: Schematic design flow of proposed multiplier

Figure 4: Layout design of proposed multiplier
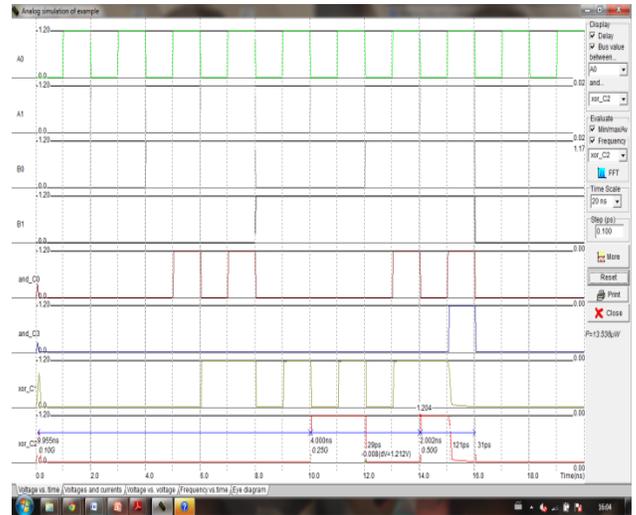

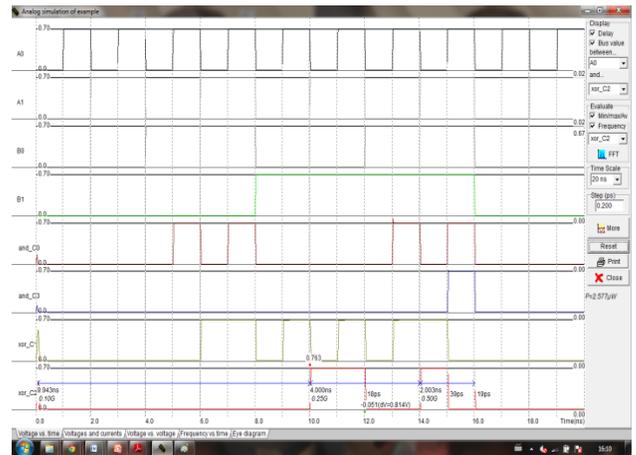Figure 5: Output of proposed multiplier using 45 nm CMOS Technology

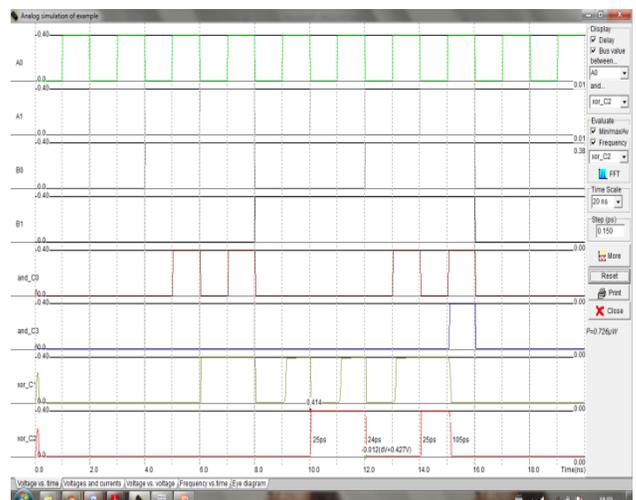Figure 6: Output of proposed multiplier using 65 nm CMOS Technology

Figure 7: Output of proposed multiplier using 90 nm CMOS Technology

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The comparative results for proposed 4-bit multipliers for 45nm, 65nm and 90 nm CMOS design technology are given in Table-1.

Table 1: Power and surface area analysis of 4-bit multiplier in different CMOS technologies

CMOS Technology / Parameters	90 nm	65 nm	45 nm
Power (in μW)	13.538	2.577	0.726
Surface Area (in μW²)	152.2	74.6	38.1

4. CONCLUSION

The proposed 4-bit Multiplier is simulated with 45 nm, 65 nm and 90 nm CMOS technologies .The performance parameters power and surface area are compared. From the results it is found that the power and surface area has been improved by 80.96% and 50.99% respectively for proposed 4-bit multiplier using the proposed logic in 65nm CMOS technology. Finally an improvement of 94.64%and 74.97% for proposed 4-bit multiplier were found using the proposed logic in 45nm CMOS technology.

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