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LOW POWER & AREA EFFICIENT LAYOUT ANALYSIS OF CMOS ENCODER

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ABSTRACT

An Encoder is a device, circuit, transducer, software program, algorithm or person that converts information from one format or code to another, for the purposes of standardization, speed, secrecy, security or compressions. Encoder is mainly used for the encoding of the data.It is having application in much area. The purpose of this paper is to design the 4 to 2 line encoder using universal gates with the help of CMOS logic and the most important. The further advanced version of the digital Encoder is 8 to 3 line Encoder, which is also proposed here. In this paper different design methodologies are used such as standard cell based design, semicustom design and full custom design of the Encoder to reduce area, power and size of the circuit. The paper analyzes and optimizes area and power of the Encoder using 45 nm technologies.

Keywords: *CMOS, Encoder, Integrated circuits, Priority Encoder.*

1. INTRODUCTION

Encoders are sensors that generate digital signals in response to movement. Both shaft encoders, which respond to rotation, and linear encoders, which respond to motion in a line, are available. When used in conjunction with mechanical conversion devices, such as rack-and-pinions, measuring wheels, or spindles, shaft encoders can also be used to measure linear movement, speed, and position. An encoder is a digital circuit that performs the inverse operation of a decoder. An encoder has 2 (or fewer) input lines and n output lines. The output lines as an aggregate generate the binary code corresponding 10 the input value [1]. An encoder is a device, circuit, transducer, software program, algorithm or person that converts information from one format or code to another, for the purposes of standardization, speed, secrecy, security or compressions. Digital Encoder is a Digital Device that uses binary number of n bit to represent a number of base ten. "CMOS" refers to both a particular style of digital circuitry design and the family of processes used to implement that circuitry on integrated circuits (chips).

CMOS circuits use a combination of p-type and n-type metal oxide semiconductor field-effect transistors (MOSFETs) to implement logic gates and other digital circuits. For the most recent CMOS feature sizes, leakage power dissipation has become an overriding concern for VLSI circuit design [2].

2. ENCODER

A Digital Encoder more commonly called a Binary Encoder take all its data inputs one at a time and then converts them into a single encoded output unlike a multiplexer that selects one individual data input line and then sends that data to a single output line or switch,. So can say that a binary encoder is a multi-input combinational logic circuit that converts the logic level "1" data at its inputs into an equivalent binary code at its output.Binary number of n bit is called Binary Coded Decimal (BCD), a coding scheme used in digital to encode informations. Encoders can be used in a wide variety of applications. They act as feedback transducers for motor-speed control, as sensors for measuring, cutting and positioning, and as input for speed and rate controls. Some examples are Door control devices, Assembly machines, Robotics, Labeling machines, Lens grinding machines, x/y indication, Plotters, Testing machines. Encoders can use either optical or magnetic sensing technology. Optical sensing provides high resolutions, high operating speeds, and reliable, long life operation in most industrial environments. Magnetic sensing, often used in such rugged applications as steel and paper mills, provides good resolution, high operating speeds, and maximum resistance to dust, moisture, and thermal and mechanical shock. There are mainly two types of encoder/decoder: memoryless and with memory. The memoryless encoder/decoder will only deal with current measurement without information about the past, while the encoder will take the past information to encoder the current measurement [3].Error Correcting Control is very important in modern communication systems. Two correcting codes that are BCH and RS codes, BCH encoder is usually implemented with **a** serial linear feedback shift register

(LFSR) architecture. In order to realize a higher data rate, parallel BCH encoder should be employed [4]. In digital audio technology, an encoder is a program that converts an audio WAV file into an MP3 file, a highly-compressed sound file that preserves the quality of a CD recording. (The program that gets the sound selection from a CD and stores it as a WAV file on a hard drive is called a ripper) An MP3 encoder compresses the WAV file so that it is about one-twelfth the size of the original digital sound file. The quality is maintained by an algorithm that optimizes for audio perception, losing data that will not contribute to perception. The program that plays the MP3 file is called aplayer. Some audio products provide all three programs together as a package.

Classification of Encoder

The Encoder is mainly of two types, rotary and linear encoder. Rotary Encoder is mainly used for Convert Angular Position into Analog or Digital Signal, for rotary motion and measuring angle, speed or velocity. Whereas the Linear Encoder Convert Linear distance movement to Analog or Digital Signal, for measuring distance travelled, positioning, location information. Some further classification is also there in these two types of the encoders, as shown in figure.

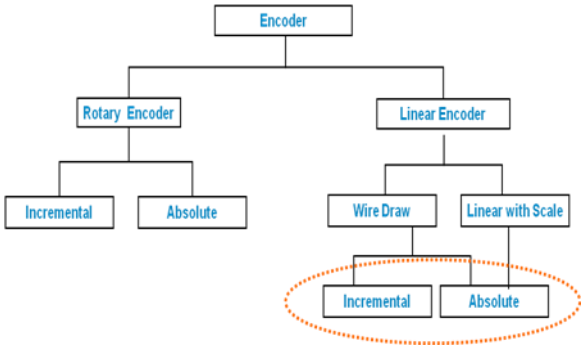

Fig.1. Encoder Tree

Convolutional Encoder

Convolutional codes are used to check and correct the errors. It can take a single bit or multiple bits as an input which gives matrix of encoded outputs. Bit sequence can be altered in Digital modulation communication systems because of noise and other external factors. To minimize the noise factor, certain additional bits are added to the encoded output which makes the bit error checking more successful and it will also yields more accurate results. This transmission of more number of bits than the original one is used to get the original signal even in the vicinity of noise. Convolution codes are considered to be best codes for controlling error and gives better performance. If 'k' are the number of input bits to be encoded, 'n' are the number of output bits encoded and 'm' are the number of shift registers used then (n, k, m) is used for expressing convolutional codes. [5]

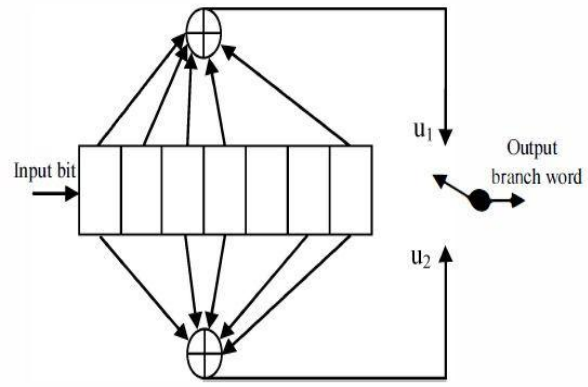

Fig. 2 Convolutional Encoder [5]

Priority Encoder (PE)

Priority encoders establish the priority of competing inputs (such as interrupt requests) by outputting a binary code representing the highest-priority active input.For producing n no. of output when there is 2^n no. of inputs. A 4-bit priority encoder. This circuit basically converts the 4-bit input into a binary representation. If the input n is active, all lower inputs (n-1 …. 0) are ignored. The circuit operation is simple. Each output is driven by an OR-gate which is connected to the NAND-INV outputs of the corresponding input lines. The NAND gate of each stage receives its input bit, as well as the NAND gate outputs of all higher priority stages. This structure implies that an active input on stage n effectively disables all lower stages n-1…..0. A common use of priority encoders is for interrupt controllers, to select the most critical out of multiple interrupt requests. Due to electrical reasons (open collector outputs) priority encoders with active-low inputs are also often used in practice.

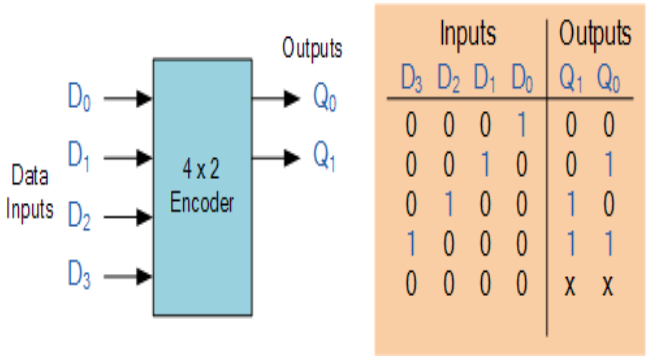

Fig.3 4 to 2 line Priorty Encoder basic building block and truth table.

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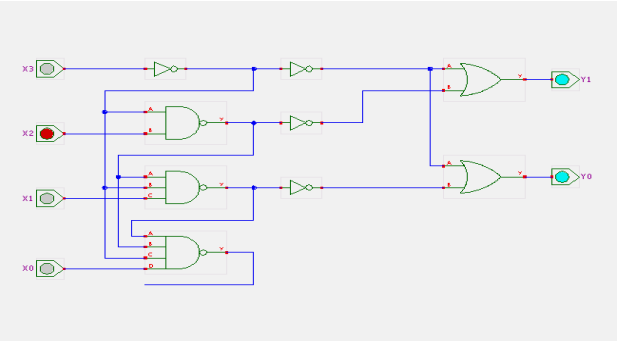
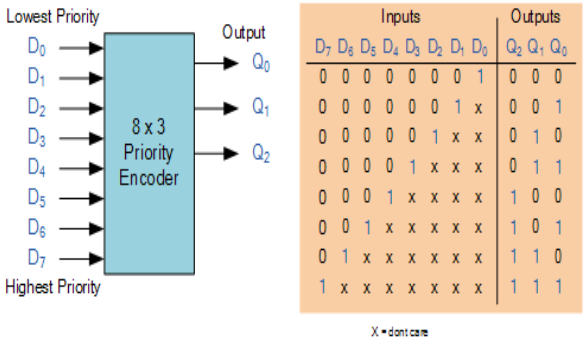


Fig.4 4 to 2 line Priority Encoder using basic building logic gates.



Inputs								Outputs		
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Q_2	Q_1	Q_0
0	0	0	0	0	0	0	1	0	0	0
0	0	0	0	0	0	1	x	0	0	1
0	0	0	0	0	1	x	x	0	1	0
0	0	0	0	1	x	x	x	0	1	1
0	0	0	1	x	x	x	x	1	0	0
0	0	1	x	x	x	x	x	1	0	1
0	1	x	x	x	x	x	x	1	1	0
1	x	x	x	x	x	x	x	1	1	1

X = dont care

Fig.5 8 to 3 Bit Priority Encoder basic building block and truth table.

$$Q_0 = \sum\left(\overline{D}_6\left(\overline{D}_4\overline{D}_2D_1 + \overline{D}_4D_3 + D_5\right) + D_7\right)$$

$$Q_1 = \sum\left(\overline{D}_5\overline{D}_4(D_2 + D_3) + D_6 + D_7\right)$$

$$Q_2 = \sum\left(D_4 + D_5 + D_6 + D_7\right)$$

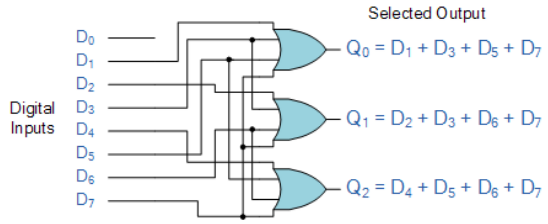


Fig.6 Digital Encoder using Logic Gates

A PE resolves the highest priority match and encodes this match location into binary format, which is used by an off-chip SRAM to retrieve the corresponding data. Typically, a PE is designed in two stages: (i) multiple match resolver (MMR), and (ii) match address encoder (MAE).

Multiple match resolver

An MMR is an *n*-bit input, *n*-bit output datapath circuit. Assuming the active-high logic convention and highest priority for the lowest address, an MMR.

Match address encoder

In the presence of multiple matches, the MMR always favors the highest priority match (lowest physical address). We designed the MAE to take advantage of this property [6]. Priority Encoder (PE) is a basic building block in many digital and mixed-signal systems. Unlike a simple encoder that allows only one of its inputs at logic-1 state, a PE does not have such restriction. It can resolve multiple logic-1 inputs and perform encoding according to the one with the highest priority [7].

3. RESULT AND SIMULATION

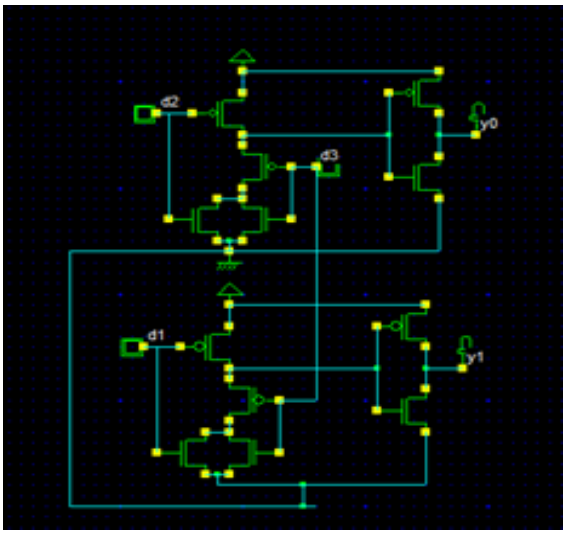


Fig.7. Schematic of 4 to 2 line Encoder using NAND gates.

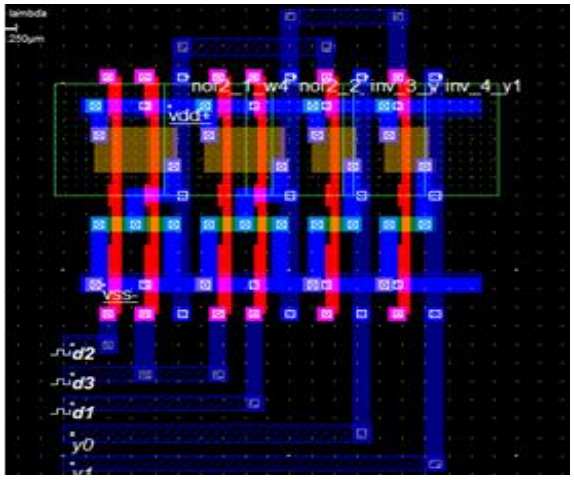


Fig.8. Standard cell layout Design of 4 to 2 line Encoder

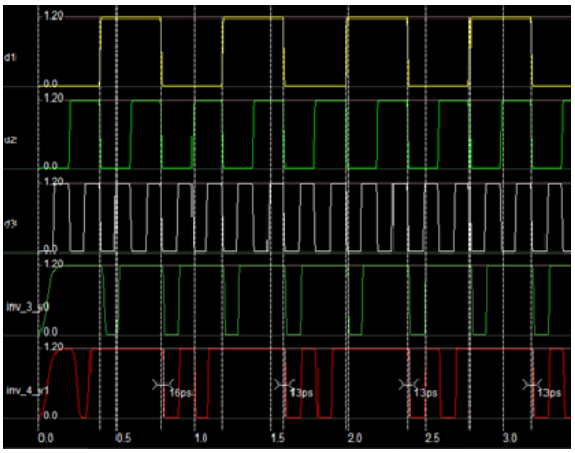


Fig.9 .Simulation Result of 4 to 2 line Encoder with standard cell design.

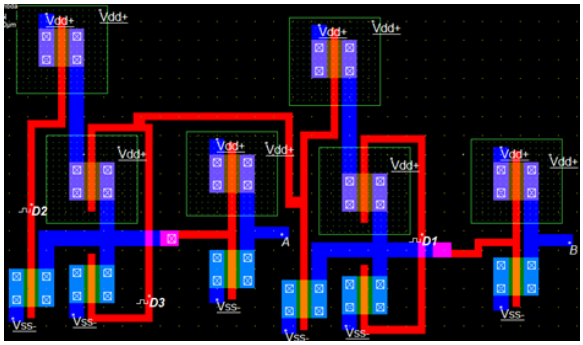


Fig.10. Semi Custom Design of 4 to 2 line Encoder

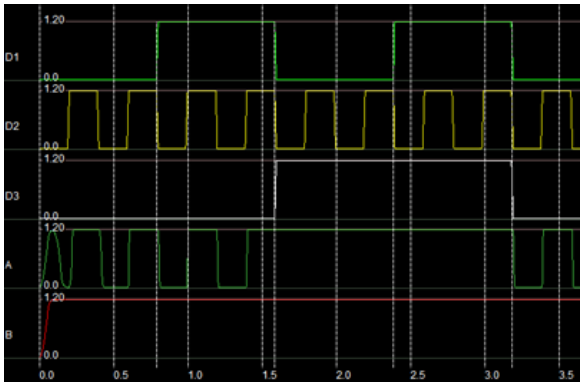


Fig.11. Simulation Result of 4 to 2 line Encoder with semi custom cell design.

4. COMPARATIVE ANALYSIS

The main parameters of consideration are area, complexity and power of the Encoder design in this paper. Table 1 shows the area and power consumption 4 to 2 line Encoder.

Table .1 Area and Power consideration

Encoder layout	Technology used	Area	Power
Standard cell based design	45 nm	32 um^2	28.37 µW
Semi custom based design	45 nm	30.4 um^2	13.82 µW

5. CONCLUSION

This analysis has proposed two different type layout design of 4 to 2 line Encoder. Standard cell based layout and semicustom based layout for the 4 to 2 line Encoder. Area, power and complexity of the different design methods are parameters taken for analysis.Table-1 shows that semi custom based layout design has 5% of reduction in the area compared to the standard cell based design. Power consumption of the semi custom layout design is 51.68 % less that standard cell based layout design.

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