International Journal of Scientific Research Engineering & Technology (IJSRET) ISSN: 2278–0882
EATHD-2015 Conference Proceeding, 14-15 March, 2015

Area Efficient Layout Design Analysis of CMOS Barrrel Shifter

Renuka Verma
Electronics & Communication department
National Institute of Teacher's Training and Research
Chandigarh

Rajesh Mehra
Electronics & Communication department
National Institute of Teacher's Training and Research
Chandigarh

Abstract
Barrel Shifter plays an important role in the data shifting and data rotation. It is having application in many areas. The Barrel Shifter is mainly use for the simplification of the data shifting. The Arithmetic and the Logical Shifters can also be replaced by the Barrel Shifter Because with the rotation of the data it also provide the application the data right, left shifting either arithmetically or logically. The purpose of this paper is to design the two bit barrel shifter using universal gates with the help of CMOS logic and the most important two 2:1 multiplexers (mux). The further advanced version of the barrel Shifter is 4 bit data shifting, which is also proposed here. In this paper different design methodologies are used such as standard cell based design, semicustom design and full custom design of the Barrel Shifter to reduce area, power and size of the circuit. The paper analyzes and optimizes area and power of the Barrel Shifter using 45 nm technologies.

Keyword- *ALU, Barrel Shifter, CMOS, Layout, Level Shifter, Microwind tool, Multiplexer, NMOS, PMOS, Shift Register, Transistor.*

1. Introduction

Data shifting is one of the important requirements of many key computer operations, from address generation to arithmetic functions. Shifting of a single data bit one field at a time can be a slow process, however. This is where a Barrel shifter comes in. Barrel Shifter is a combinational circuit with n data inputs and n data outputs with control inputs that specify the shifting of the input data as the output and bit barrel shifter requires n, n bit multiplexers. But n-bit barrel shifter requires n number of n-bit multiplexers. If n is increased the circuit complexity also increases i.e., circuit over head, it leads to occupy more area and high power consumption and also shows the effect on speed of the operation [1]. The latest technology used for constructing integrated circuits is Complementary metal oxide semiconductor (CMOS). The technology is being used in various digital and analog logic circuits such as image sensors (CMOS sensor), data Converters and highly integrated transceivers for many types of applications [2]. Barrel shifter is often used for shifting operation like shift right logical, shift left logical, shift left arithmetic, shift right arithmetic, right rotate, and left rotate. The designing of the Barrel Shifter can be done by using multiplexers. So to design the shifter, we have to design multiplexer first. Generally 2:1, 4:1, 8:1 mux trees are used for designing of the shifter. In this paper we have designed the barrel shifter using 2:1 mux tree and 45 nm technology. The result comprises the comparison between different methodologies to reduce the Power consumption in ALU design [3].A Shifter is most useful for arithmetic operations since shifting is equivalent to multiplication by powers of two. Floating point arithmetic is the example of the shifter. Presently there are large number of shifters are in use. The simplest shifter is the shift register, which can shift by one position per clock cycle, but generally there is a need to shift several bits in one cycle and to vary the length of the shifts. The Shifters can be classified as Logical Shifter Arithmetic Shifter Barrel Shifter Funnel Shifter and Level Shifter. Logical Shifter can shift the data to left or right. Data is shifted towards left and right by given logic and the empty places are filled by 0's. Arithmetic Shifter is same as the logical shifter in case of left shifting. But in case of right shifting the empty places or the most significant bits will be as same as the sign bit. Barrel Shifter can perform n bit shifts in a single combinational function or in a single clock cycle and having efficient layout. Barrel Shifter is also known as Rotator because it rotates the data in a cycle such that the empty spots are filled by the bits shifted off the other hands. A funnel shifter can do all six types of shifts which are performed by previously mentioned shifters. Level shifters are used to convert logical signal from one voltage to another voltage. Apart from this level shifters are used at the pad ring and core of chip interface where low voltage signal from chip core are shifted to high voltage [4].

2. Barrel Shifter

A Barrel Shifter is part of a microprocessor CPU which can typically specify the direction of shift left or right,

the type of shift circular, arithmetic, or logical and the amount of shift (typically 1 to n-1 bits, but sometimes 1 to n bits). Barrel Shifters are generally used for the digital signal processors and general purpose processors to manipulate the data. A barrel shifter is a digital circuit that can shift a data word by a specified number of bits in one clock cycle. It can be implemented as a sequence of multiplexers (mux), and in such an implementation the output of one mux is connected to the input of the next mux in a way that depends on the shift distance.

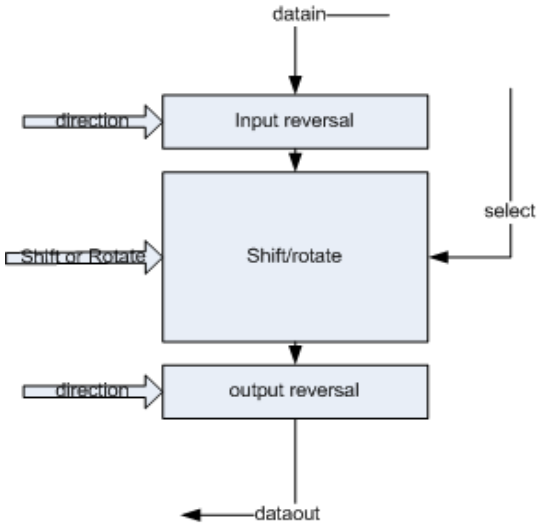

Fig.1 Basic block diagram of Barrel shifter

Barrel Shifter accepts 2n data inputs and n control signals, producing n data outputs. [5]

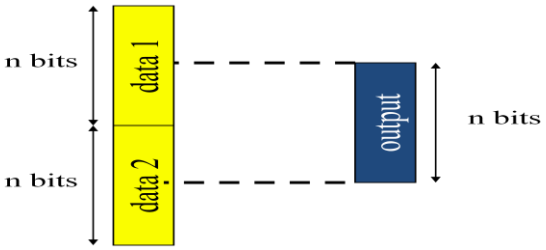

Fig.2 How Barrel shifter performs shifts and rotates [5]

The Barrel Shifter control lines run vertically, the input data run diagonally upward through the system and the output data run horizontally [5].The shifting of the data in the Barrel Shifter can be as per the user requirement. The Barrel Shifter is commonly used shifter architecture. One of the important reasons behind the wide usage of this architecture is the fact that it can perform multi-bit shifts in a single operation within one clock cycle.

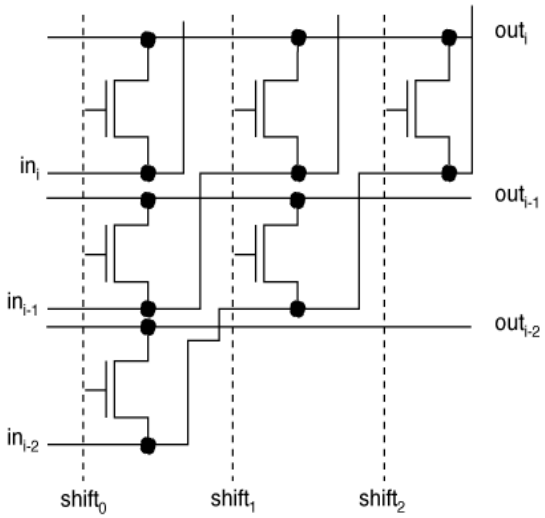

Fig.3 Schematic of the Barrel shifter

In addition, the area of the barrel shifter is also reasonably small. [6]. Barrel Shifter consists of an array of transistors, in which the number of rows equals the word length of the data, and the number of columns equals the maximum shift width. The control wires are routed diagonally through the array. The design of the barrel shifter is almost symmetric and can be done using repetitive combinational logic blocks. 2:1 multiplexer can be effectively used to design n bit barrel shifter. Fig. shows the block schematic of a 2X2 barrel shifter using four 2:1 multiplexers. If each multiplexer block is optimized for energy dissipation then the simulation time of the entire barrel shifter is reduced by a factor of $n\log_2 n$ times because simulation of only one multiplexer is enough to estimate the overall energy dissipation and delay.[7]

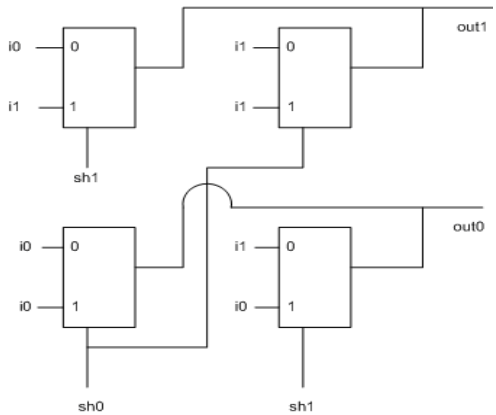

Fig.4 Multiplexer based 2X2 barrel shifter [7]

Today's integrated circuits have a growing need for speed, area, and power. Despite many advantages, CMOS suffers from increased area, more power

dissipation and correspondingly increased capacitance and delay, as the logic gates become more complex. Ratioed circuits use weak pull-up devices and stronger pull down devices. They reduce the input capacitance and hence improve logical effort by eliminating large PMOS transistors loading the inputs, but depend on the correct ratio of pull-up to pull-down strength [8]. 2:1 multiplexer can be effectively used to design n bit Barrel shifter, if each multiplexer block is optimized for energy dissipation. [9]

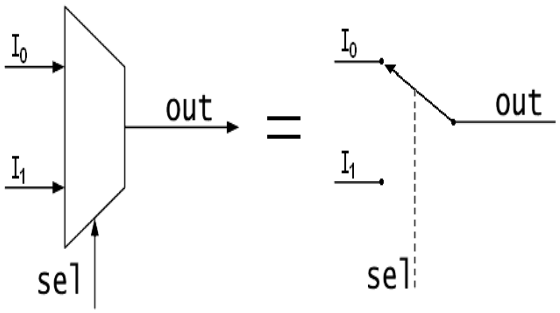

Fig.5 Basic building of 2: 1 multiplexer

A barrel shifter is often implemented as a cascade of parallel 2×1 multiplexers.

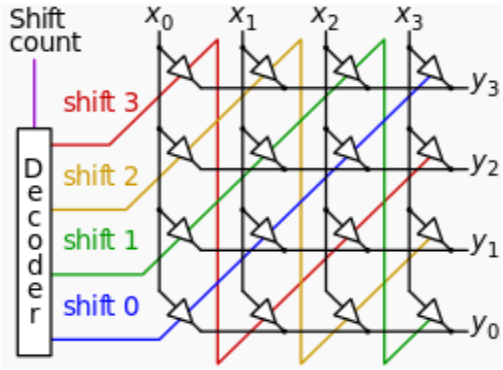

Fig.6 Schematic of a 4 bit crossbar Barrel Shifter, X denotes input bits and *y* denotes output bits.

Rotate and Shift Operation of Barrel Shifter

Barrel shifter can mainly perform shift right logical, shift left logical, shift right arithmetic, shift left arithmetic, rotate right and rotate left operations of shifting. The left and right operation is implemented through inversion of the input and output vectors, so the basic multiplexing function can perform both operations. The number of multiplexing stages is relative to the width of the input vector.

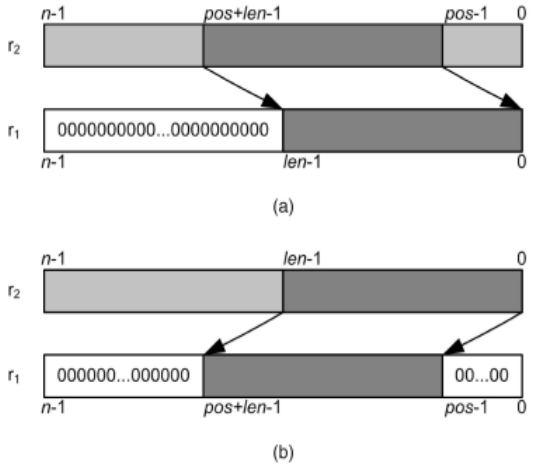

Fig.7 (a) extr.u r_1 ¼ r_2, pos, len. (b) Dep.z r_1 ¼ r_2, pos, len. [10]

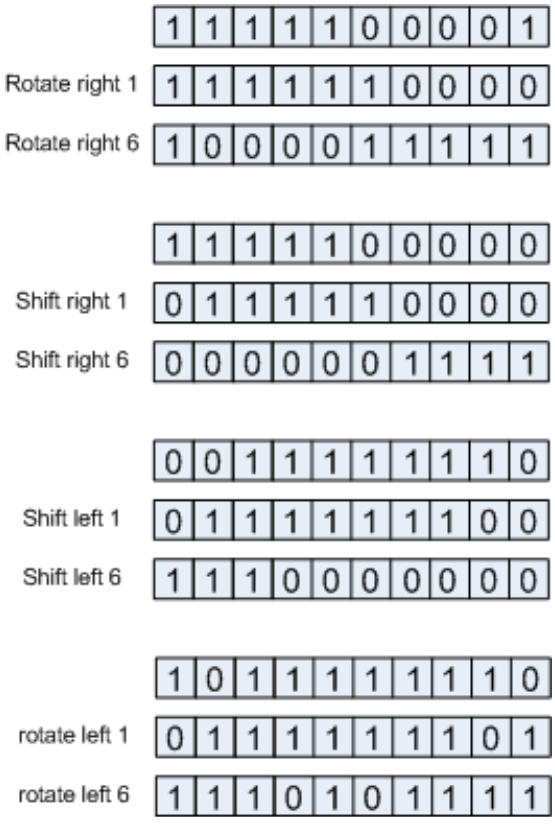

Fig.8 Shift and rotate operation of Barrel Shifter

The rotate is a cyclic shift either to the left or right. It means when the bits are shifted into the data vector on one side, they are shifted to the data vector on the other side. The positions of the bits can vary their positions because the bits are routing from input to the output [5]. The rotate operation is a shift where the bit which is shifted out of the vector MSB is inserted at its LSB.

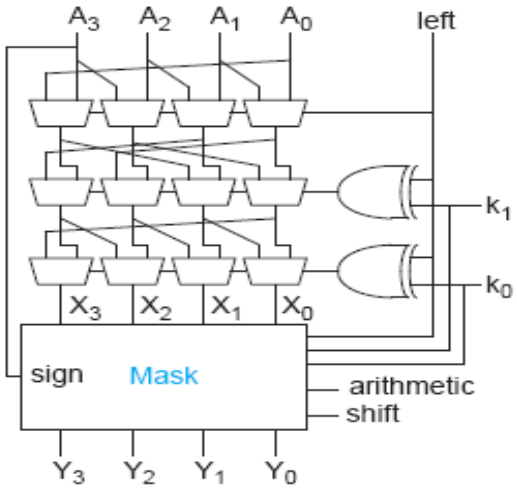

Fig.9 Right/Left rotates and shift operation

Shifting operation of Barrel Shifter

The shifting operation of the barrel shifter is of two types. One is right shift and the second one is left shift. The right and left specify the direction of the shifting. The shift operation inserts 0 values for each shift operation. The input vector is shifted in the selected direction according to the number of bits in the select indication.

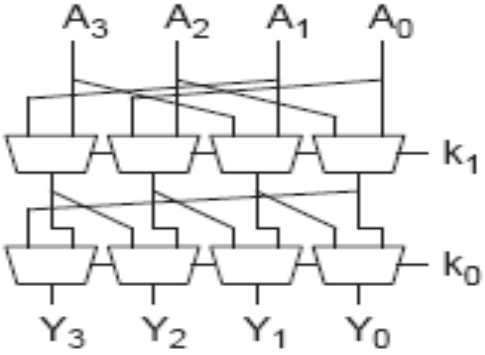

Fig.10 Right shift operation

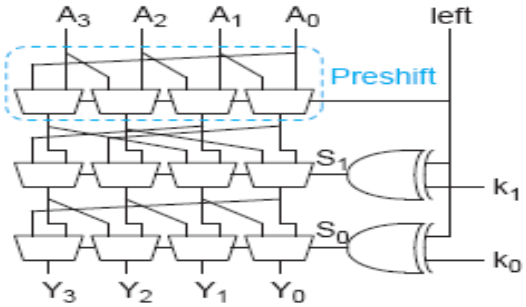

Fig.11 Right/Left shift operation

3. Simulation and Result

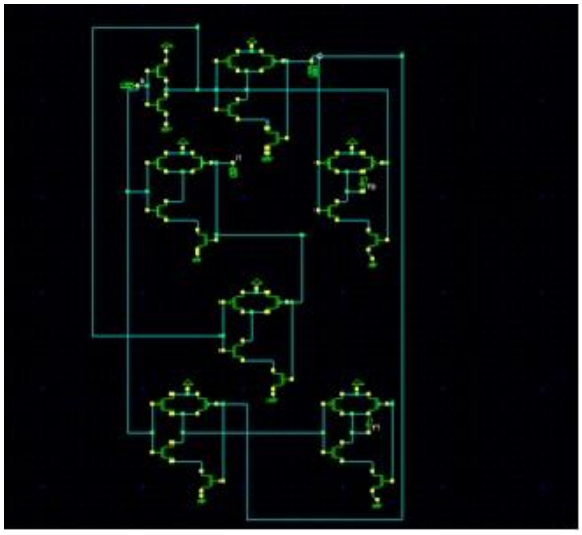

Fig.12 Schematic of 2 bit Barrel Shifter using 2:1 multiplexer using NAND gates.

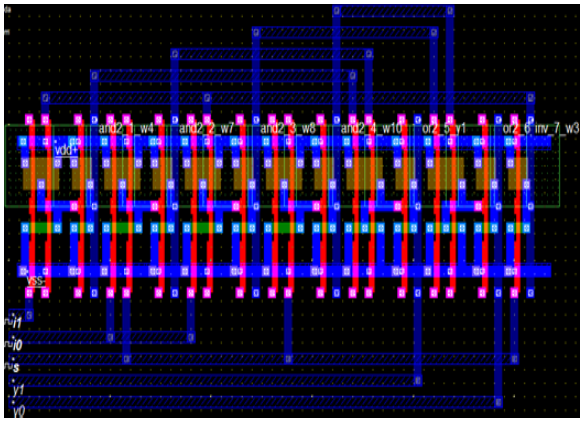

Fig.13 Standard cell layout Design of 2 bit Barrel Shifter

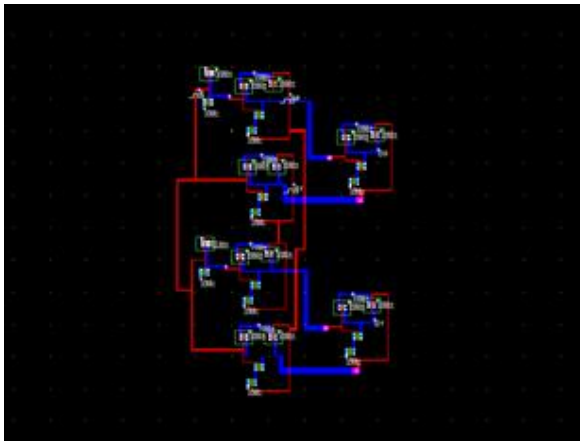

Fig.14 Semi Custom Design of 2 bit Barrel Shifter

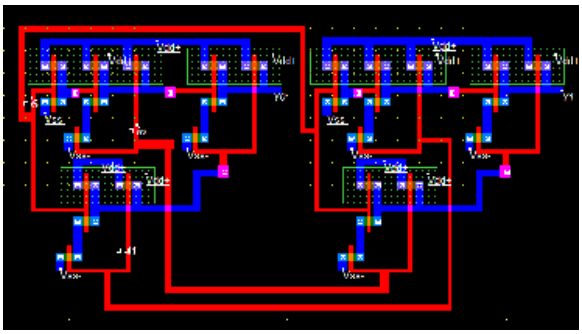

Fig.15 Full Custom Design of 2 bit Barrel Shifter

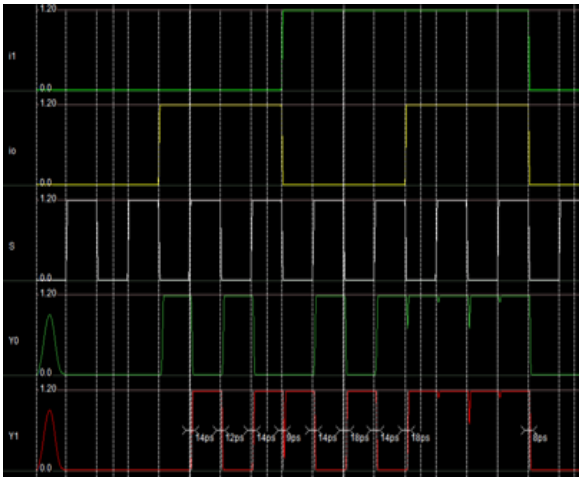

Fig.16 Simulation Result of 2 bit Barrel Shifter

4. Comparative Analysis

The main parameters of consideration are area, complexity and power of the 2 bit Barrel Shifter design in this paper. Table 1 shows the area and power consumption of 2 bit Barrel Shifter as rotator using 2 to 1 multiplexer circuit.

Table.1 Area and Power consideration

Barrel Shifter Layout	**Technology Used**	**AREA**	**POWER**
Standard cell based design	45 nm	18.4 um^2	17nW
Semi custom based design	45 nm	15 um^2	1.768 µW
Full Custom Design	45 nm	9.6 um^2	0.994 µW

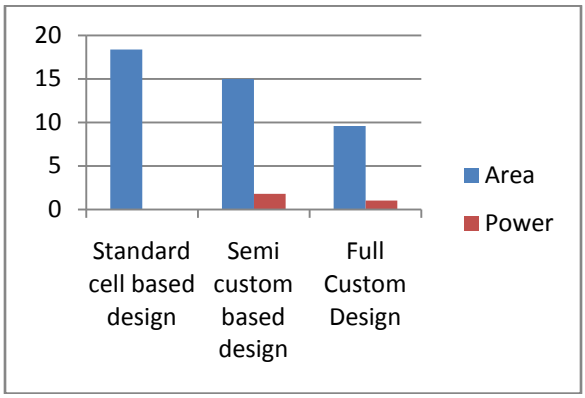

Fig.17 Area and Power consideration of 2 bit Barrel Shifter

5. Conclusion

This analysis has proposed three different type layout design of 2 bit barrel shifter. Standard cell based layout, semicustom based layout and full custom layout are developed for the 2 bit barrel shifter. Area, power and complexity of the different design methods are parameters taken for analysis. Table.1 shows that semi custom based layout design has 18.47% of reduction in the area compared to the standard cell based design. Full custom design has 47.826 % of reduction in the area compared with the standard cell and 43.778 % reduction in the area compared than semicustom based design layout. Power consumption of the full custom layout design is 43.77 % less that semicustom based layout design.

Acknowledgement

The authors would also like to thank Director, National Institute of Technical Teacher's Training & Research, Chandigarh and Director, Roorkee Institute of Technology, Roorkee, India for their constant inspirations and support throughout this research work.

References

[1] D A Tatajee, K Rajesh."Semi custom Implementation of Area Efficient Barrel shifter", International Journal of Advanced Computing, Engineering and Application, Vol. 1, pp.112-114, December 2012.

[2] Pooja Singh, Rajesh Mehra, "Design Analysis of XOR Gates Using CMOS & Pass Transistor" International Journal of Engineering Science Invention

Research & Development, Vol. 1 Issue 1, pp.21-25, July 2014.

[3] Dhananjay Jadhav, Mithilesh Muley, Manglesh Ashtankar, "Vlsi Design of Barrel Shifter Using Complementary and Pseudo Nmos Logic", 4th IRF International Conference, pp.170-172, March 2014.

[4] Shilpa Thakur, Rajesh Mehra "CMOS Design and Single Supply Level Shifter Using 90nm Technology" Conference on Advances in Communication and Control Systems, pp.150-153, 2013.

[5] Wayne Wolf, "Modern VLSI Design (System on chip Design)", Pearson Education, pp. 319-321.

[6] Sabyasachi Das, Sunil P. Khatri."Timing-Driven Decomposition of a Fast Barrel Shifter" IEEE, pp.574-577, 2007.

[7] Prasad D Khandekar, Dr. Mrs. Shaila Subbaraman, Venkat Raman Vinjamoori, "Quasi-Adiabatic 2X2 Barrel Shifter" Fourth International Conference on Industrial and Information Systems, ICIIS, IEEE, pp.321-324, December 2009.

[8] Akhilesh Verma, Rajesh Mehra, "Design and Analysis of Conventional and Ratioed Cmos Logic Circuit" IOSR Journal of VLSI and Signal Processing Vol.2, pp. 25-29, April 2013.

[9] Prasad D Khandekar, Dr. Mrs. Shaila Subbaraman, "Low Power 2:1 MUX for Barrel Shifter" First International Conference on Emerging
Trends in Engineering and Technology, IEEE, pp.404-407, July 2008.

[10] Yedidya Hilewitz, Ruby B. Lee, "A New Basis for Shifters in General-Purpose Processors for Existing and Advanced Bit Manipulations" IEEE Transactions on Computers, VOL. 58, pp.1035-104, August 2009.

Authors

Renuka Verma received the Bachelors of Technology degree in Electronics and Communication Engineering from Govind Ballabh Pant Engineering College, H.N.B, Garhwal, University, Shrinagar, India in 2009, and persuing the Masters of Engineering degree in Electronics and Communication Engineering from National Institute of Technical Teacher's Training & Research, Punjab University, Chandigarh, India.

Rajesh Mehra received the Bachelors of Technology degree in Electronics Communication Engineering from National Institute of Technology, Jalandhar, India in 1994, and the Masters of Engineering degree in Electronics and Communication Engineering from National Institute of Technical Teacher's Training & Research, Punjab University, Chandigarh, India in 2008. He is pursuing Doctor of Philosophy degree in Electronics and Communication Engineering from National Institute of Technical Teacher's Training & Research, Punjab University, Chandigarh, India. He is an Associate Professor with the Department of Electronics & Communication Engineering,, National Institute of Technical Teacher's Training & Research, Ministry of Human Resource Development, Chandigarh, India. His current research and teaching interests are in Signal and Communications Processing, Very Large Scale Integration Design. He has authored more than 175 research publications including more than 100 in Journals. Mr. Mehra is member of IEEE and ISTE.