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Design Analysis of 1-bit CMOS comparator

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ABSTRACT
In this paper three different techniques are used for designing a 1-bit comparator and then a comparison is made about area and power consumption. First one is autogenerated comparator, second one is semi-custom comparator and the third one is fully custom design. Today's technology demands to develop various new design methodologies to reduce the area and power consumption as small saving in area and power of a circuit yield a large overall saving. From the given comparison, we found that full-custom design saves about 50%in area and 35%in power consumption when compared with autogenerated design and saves 37% in area and 98% power saving when compared with semi-custom design.

***Key Words**: CMOS, Comparator, low power, less area.*

1. INTRODUCTION
The comparator is an electronic circuit which compares the voltage of a signal to another signal or a reference voltage and outputs a binary signal based on comparison. The comparator is basically 1-bit analog-to digital convertor.Fig.1 shows general block diagram and fig.2 shows the symbol of low voltage comparator

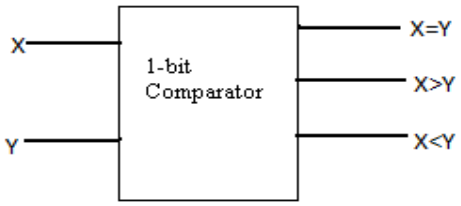

Fig.1 Block diagram of a comparator.

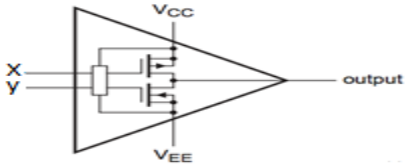

Fig.2 Symbol of a low power comparator

Comparator circuit finds frequent application in measurement and instrumentation circuits. The comparator is a significant part of most of the analog-to-digital (ADC) convertor. The type and architecture of the comparator have significant impact on the performance of the target application. The speed and resolution of an ADC is directly affected by the comparator input offset voltage, the delay and input signal range. Some basic application of comparators is analog-to digital conversion, function generator, signal detection and neural network etc. [1, 2]

Magnitude comparator is basically a combinational circuit that compares two numbers, X and Y and determines their relative magnitude i.e.$> Y$, X=Y, X$< Y$.Here we want comparison between two variables and producing an output when any of the above three conditions are achieved. There are different approaches to design CMOS comparator, each with different speed, power consumption and area. The following study gives an overview of the basic 1-bit comparator performance in designing with different techniques in terms of power consumption and area using 45nm CMOS technology.

First of all we have to design a 1-bit comparator. X and Y are two inputs and three outputs X$> Y, X = Y, X < Y$ and only one of the three outputs would be high accordingly if X is greater than or equal to or less than Y. The truth table of 1-bit comparator is shown in fig.3

Input		Output		
X	Y	$X > Y$	X=Y	X$< Y$
0	0	0	1	0
0	1	1	0	0
1	0	0	0	1
1	1	0	1	0

Fig.3 Truth table of 1-bit comparator

We have equation of 1-bit comparator. We draw the schematic diagram by the use of this equation. Now we get equations using k-map using truth table of 1-bit comparator for f(X$> Y$), $f(X = Y), f(X < Y)$.

X>Y

Y / X	0	1
0	0	0
1	1	0

Equation is X>Y=X.$\bar{Y}$

X<Y

Y / X	0	1
0	0	1
1	0	0

Equation is X<Y=$\bar{X}$.Y

X=Y

Y / X	0	1
0	1	0
1	0	1

Equation is f(x=y) =$\bar{X}.\bar{Y}$+X.Y

2. CMOS DESIGN TECHNOLOGY

Silicon CMOS technology has become the dominant fabrication process for relatively high performance and cost effective VLSI circuits. CMOS design technology is extensively used in almost all electronics and digital processing circuit. The current trend in designing is to use a circuit which require less area, consumes less power and provides high speed. Since CMOS consumes less power and provides a moderate speed, it is considered as the best alternative component for designing a digital circuit [3].The CMOS circuit is shown in fig.3.

The triangle at the top indicates Vdd and the bottom sign indicates the GND. When the input A is '0', the nMOS transistor is OFF and the pMOS transistor is ON. Thus the output is pulled up to'1' since it is connected to Vdd but not to GND. Conversely, when A is '1', the NMOS is ON and the PMOS is OFF, and the output is pulled down to'0'.Here CMOS invertor and NAND gates are used to design AND gate [4]

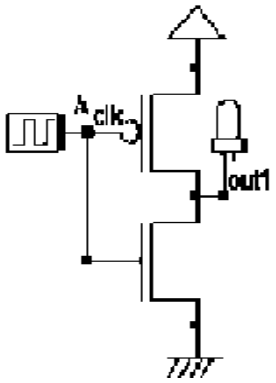

Fig.3 CMOS circuit

A design often requires a compromise between conflicting requirements. The invertor gain can be improved by slightly increasing the length of the transistor at the expense of input loading capacitance. If the width of the PMOS is increased with respect to NMOS the Q-point of the transfer characteristic moves towards midpoint but increases the input characteristic which results in the reduction of gain [5].

Here we use Microwind software to draw the layout of the CMOS circuit. The Microwind 3.1 is a comprehensive solution for designing and simulating microelectronic circuits at layout level with different modules for layout designs up to 45nm, schematic editor, mixed signal and analog simulator, Verilog and SPICE support. We design and simulate 1-bit comparator with three different techniques. In digital systems, comparison of two numbers is an arithmetic operation that determines if one number is greater than, equal to, or less than the other number.Figure.3 shows the 1-bit magnitude comparator.

In CMOS designing gate width and length are two major parameters which affect the performance of the device. Within the gate depletion (Wd), the mobile carriers are swept away by the applied gate field. The maximum gate depletion width attains at the onset of the inversion. At this point electron concentration at the surface is equal to the hole concentration of the substrate. Now the surface potential (ψ_s) becomes

$$\psi_s = 2\psi_B$$

Where $\psi_B = KT/q \ln\frac{N_a}{N_i}$ and N_a is substrate doping concentration. For uniformly doped concentration

$$W_{dm} = \sqrt{\frac{4\epsilon_{si} KT/q \ln\frac{N_a}{N_i}}{q^2 N_a}}$$

Where ϵ_{si} is the permittivity of silicon material. Reduction inW_{dm}can improve the short channel effect but requires a tradeoff between substrate sensitivity and sub threshold Slope. To reduce the gate- controlled depletion width, a retrograde channel doping is required for a channel length L≤0.2μm.

Another feature of the MOSFET is the gate length which is patterned by the lithography and etching. By using optical lithography we can reduce the feature size through reduction in light wavelength [6].

3. LAYOUT TECHNOLOGY

Silicon is the most widely used material for the fabrication of the IC.IC industry researcher predicts that the popularity of silicon will sustain in future CMOS integrated circuit can be built on silicon wafer by using simple and inexpensive techniques. The creation of a circuit on silicon wafer involves two major types of operation: doping impurities into selected wafer region to change electrical properties and depositing patterned materials on the wafer surface [7].

In our designing we used DSCH.3.1 and Microwind software tools. DSCH is software for logic design. Based on primitives, a hierarchical circuit can be built and simulated. It also includes delays and power consumption evaluation. Microwind is a tool for designing and simulating circuit at layout level .This tool is featured with full editing facilities like copy, cut paste, duplicate, move etc. In this tool we can also view the 2D cross-section, 3D process viewer and an analog simulator [8].

4. LAYOUT AND SIMULATION RESULTS

Fig.4 is the schematic logic design built on DSCH and also checked by using LED's .Fig.5 is the 1-bit comparator design using NMOS and PMOS transistors on DSCH. Fig.6 is the autogenerated layout of the design shown in fig.5 and its simulation is also shown in fig.7.Fig.8 is the semi-custom layout built on Microwind and its simulation is shown in fig.9.Full-custom layout is shown in fig.10 and its simulation is shown in fig.11.

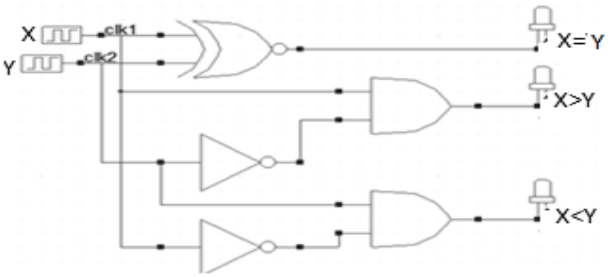

Fig.4 Schematic of 1-bit comparator

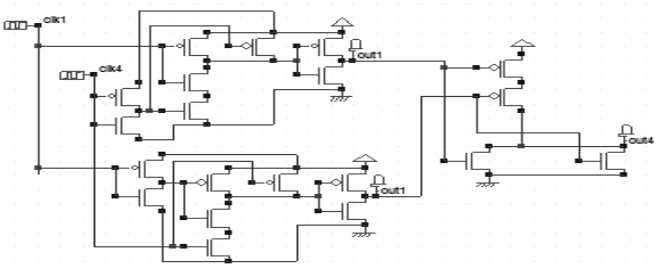

Fig.5CMOS design of 1-bit comparator using pass transistor.

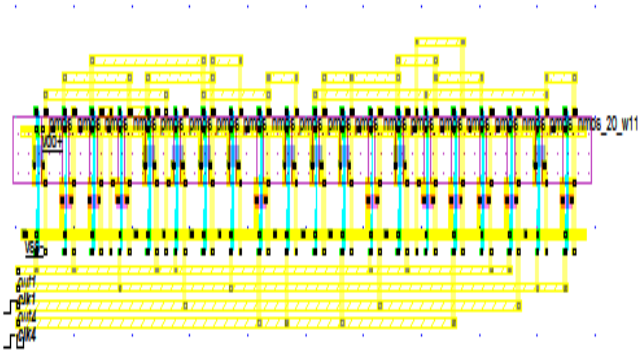

Fig.6Auto generated layout of the comparator.

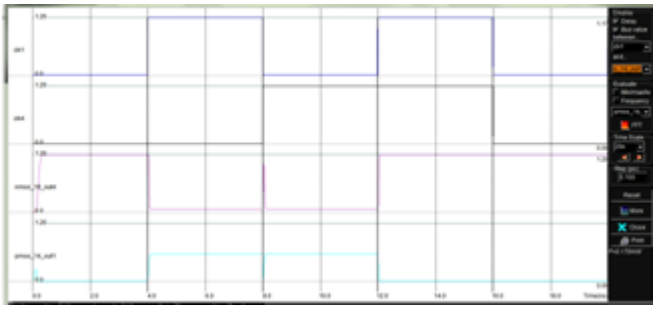

Fig.7 Timing diagram of autogenerated 1-bit comparator

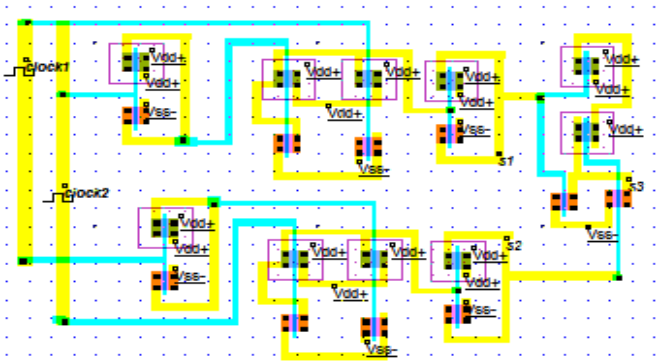

Fig.8 Semi-custom layout of the comparator.

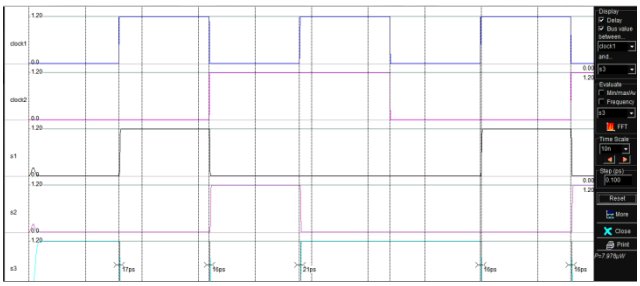

Fig.9 Timing diagram of semi-custom 1-bit comparator

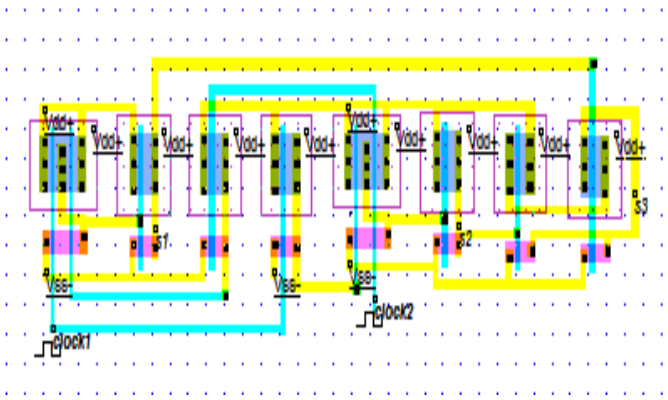

Fig.10 full-custom layout of the comparator.

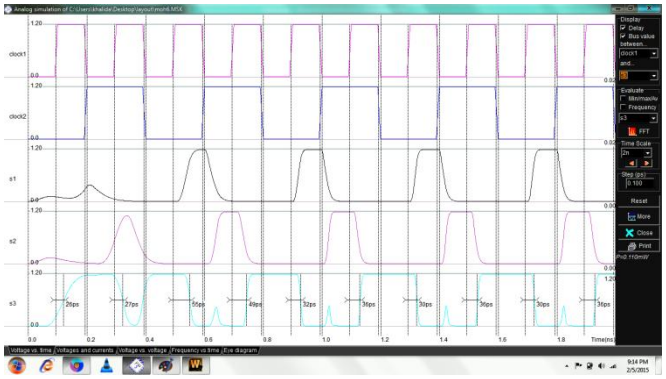

Fig.11 Timing diagram of full-custom 1-bit comparator

5. ANALYSIS AND COMPARISON

Analysis and comparison of different layouts of comparator are shown in table. In first layout process, the circuit is designed from the schematic and a Verilog file is generated using DSCH 3.1.This Verilog file is compiled and simulated in Microwind 3.1.which results in autogenerated layout. In second layout we used semi-custom design approach in which the NMOS and PMOS modules are already built by the software tool and connections are made by the designer manually and a simulation is obtained. In the third layout we use full-custom design approach in which the NMOS and PMOS transistor module and their connections all are designed manually.

Parameters	Autogenerated comparator	Semi-custom comparator	Full-custom comparator
Width	24.9μm	13.8μm	16.8μm
Height	6.6μm	9.3μm	4.8μm
Area	164.3μm^2	127.9μm^2	79.6μm^2
Power	0.170mW	9.943mW	0.110mW

6. CONCLUSION

This paper has described three different designs for CMOS 1-bit comparator and their simulation. Autogenerated approach is easy to design but takes more area and consumes less power than semi-custom design approach. Semi-custom design takes less area but consumes much more power than autogenerated design. Finally full-custom design takes less area and also consumes less power than both autogenerated and semi-custom design. Final results shows that full-custom design is more area and power efficient as it takes only 50 % of the area and saves 35 % of power consumption when compared with autogenerated design and takes only 37 % of area and saves 98 % of power when compared with semi-custom design.

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