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Area and Power Efficient Layout Design of CMOS Schmitt Trigger

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ABSTRACT
Schmitt triggers are extensively used in digital as well as analog systems to filter out any noise present in a signal line and produce a clean digital signal. This circuit is used in many instrumentation and test measurement systems. Schmitt trigger devices are used in open loop configuration for noise immunity and closed loop positive feedback configuration to implement the multivibrators. In this paper a Schmitt trigger and its layout has been designed using PMOS and NMOS transistors. The result has been compared in terms of power consumption and surface area. The simulated result shows that an auto generated Schmitt trigger consumes 37% more power and 22.78% more surface area than the semi-custom layout of Schmitt trigger.

Key Words: *Comparator circuits, CMOS, Filter, Schmitt Trigger, Threshold current, VLSI*

I. INTRODUCTION

In the earlier period, the VLSI designers were more bent toward the performance and area of the circuits [1]. Cost and Reliability also gained core importance whereas power consumption was a peripheral consideration for them. In recent years the power is an important parameter in comparison to area and speed [2]. Power consumption is one of the basic constraints in any integrated circuit. There is always a trade-off between power and performance [3]. Power consumption of CMOS consists of dynamic and static components [4]. Dynamic power is consumed when transistors are being switched, and static power is consumed regardless of transistor switching. Modern digital circuit consists of logic gates implement in the CMOS. Power consumption has two components one is dynamic power and the other is leakage power [5]. Dynamic and leakage power contributes the total power consumption. Traditionally static power consumption has been overshadowed by dynamic power consumption, but the transistor size continues to shrink. Dynamic power dissipation is proportional to the square of the supply voltage. In deep submicron process supply voltages and threshold voltages for CMOS transistors have greatly reduced. This reduces the dynamic power dissipation [6].

II. SCHMITT TRIGGER

VLSI circuit is used for increasing number of portable application with limited amount of power available [7]. Schmitt Triggers are used in buffer, sub threshold SRAM [8], sensors [9] and pulse width modulation circuits. A Schmitt trigger is a comparator circuit that incorporates positive feedback [10]. If the input is higher than a certain chosen threshold, the output is high and when the input is below another chosen threshold, the output is low. If the input is between the two, the output retains its value [11-12]. The circuit is named a trigger because the output retains its value until the input changes sufficiently to trigger a change [13]. This dual threshold action is termed as hysteresis. In fact Schmitt trigger is a bistable multivibrator. Fig.1 shows the block diagram of a Schmitt trigger circuit. It is a system with positive feedback in which the output signal feedback into the input to cause the amplifier A to switch from one saturated state to other if the input crosses a threshold value. In the given fig.1, A is the amplifier gain and B is the transfer function.

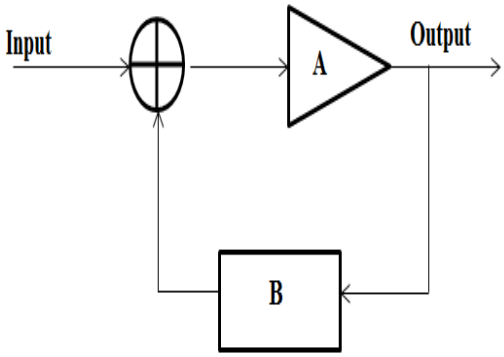

Fig.1: Block diagram of a Schmitt Trigger

III. LAYOUT DESIGN

A commonly used Schmitt trigger design is shown in fig.2. This structure has 3 PMOS and 3 NMOS transistor along with positive feedback.

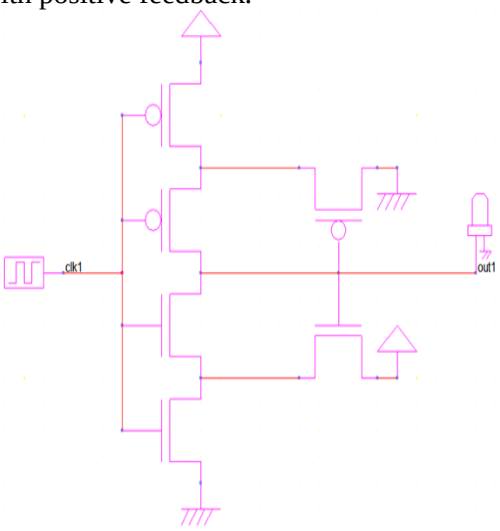

Fig. 2: Schematic diagram of Schmitt trigger using CMOS

This technique uses aspect ratio W/L=5 for PMOS and NMOS transistor and 90nm technology. The layout design rule describes how the small feature can be and how closely they can be packed in particular manufacturing process. Different logical layers are used by the designer to generate the layout of the circuit. There are specific layers for metal, contacts and diffusion areas and polysilicon. Fig. 3 shows the auto generated layout design using DSCH and Microwind tools using λ based design rule.

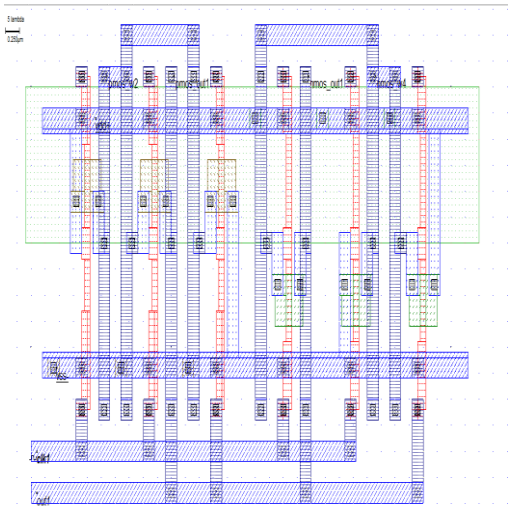

Fig. 3: Autogenerated Schmitt trigger

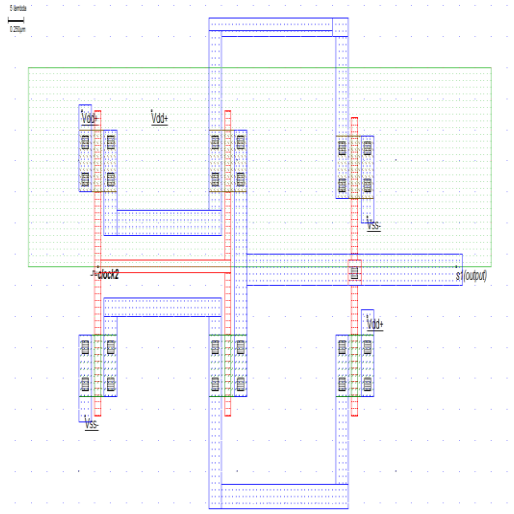

Fig.4: Semi-custom Design of Schmitt trigger

Fig. 4 shows the semicustom Design of schmitt trigger circuit using PMOS and NMOS transistor of 90nm technology. The aspect ratio of PMOS and NMOS is W/L=5

IV. SIMULATED RESULTS

Fig. 5 and fig.6 show the voltage versus time output of an auto generated and semi-custom layout of Schmitt trigger circuit. The time scale is 5n and step (PS) is 0.100

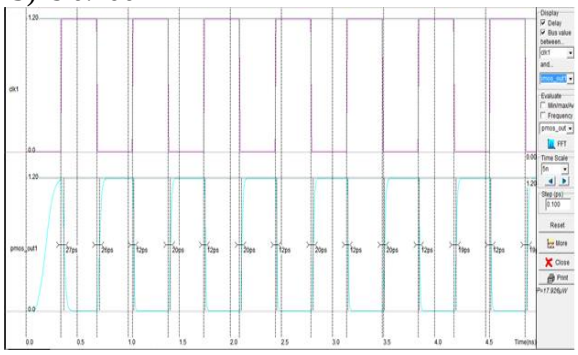

Fig. 5: Voltage versus time (auto generated)

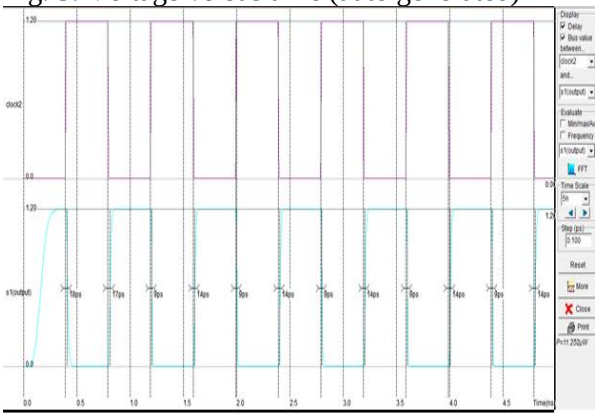

Fig. 6: Voltage versus time (semi-custom design)

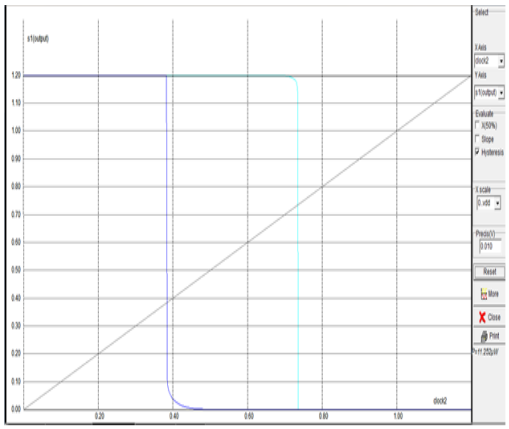

Fig. 7: Voltage versus voltage (hysteresis)

Table1, indicate the comparison of an auto generated layout and semi-custom layout of Schmitt trigger.

Schmitt Trigger / Parameter	Auto generated layout	Semi-custom layout
Power	17.926 µw	11.25 µw
Surface Area	37.3µm^2	28.8 µm^2

V. CONCLUSION

In this paper a Schmitt trigger and its layout has been designed using PMOS and NMOS transistors. In this design 3 PMOS, 3 NMOS transistors and 90nm technology with DC level 1.2 V has been used. The result has been compared in terms of power consumption and surface area of an auto generated and semi-custom layout of Schmitt trigger. The simulated result shows that an auto generated layout covers 37.3µm^2 and semi-custom layout covers 28.8 µm^2 surface area. The simulated result also shows that an auto generated layout consumes 17.926 µw power and semi-custom layout consumes 11.25 µm power.

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