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Low power and Area Efficient Full Adder Layout Design Using 32 nm CMOS Technology

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Abstract
Full adders are very important component in designing of many sophisticated hardware circuits and wide variety of processors. In the technological environment it has become essential to develop various new design technologies to reduce the power and area consumption. In this paper the full adder has been designed with the help of 10 transistors using 32 nm CMOS technology. Two different layout design techniques have been discussed in this paper i.e.; auto generation technique and semi-custom layout design. Designed layouts are compared in terms of power and area consumption. The semi customized full adder layout has shown the improvement of 35%- 58.53% in power consumption and 44%- 51.48% in area.

Key Words: *CMOS, Full adder, Power Dissipation, Very Large Integrated Circuit, XOR, XNOR.*

I. INTRODUCTION
Portable devices like PDAs, cell phones, etc., demand high speed processing capabilities that also consume less power. Power dissipation is increasing as number of transistors increases on a single chip[1]. The electronics industry has achieved a phenomenal growth over the last couple of decades, mainly due to the rapid advances in integration technologies (IC) and large scale systems design. The level of integration as measured by the number of logic gates in a monolithic chip. The full adder is one of the most essential components of any hardware or processor, as it is used in arithmetic logic unit (ALU), in the floating-point unit, and for address generation in case of cache or memory access.

Many full adder cells have been proposed [2]. The transmission gate CMOS full adder cell uses transmission gate logic. It realizes the complex function with a reduced number of CMOS transistors. The transmission gate full adder cell is faster than the CMOS full adder. The basic full adder has three inputsA (operand 1), B (operand 2) and Cin (input carry) and two outputs which are sum and Cout (output carry). The logical expression for the outputs of adder can be given by the following equations:

$$SUM = A \oplus B \oplus Cin \quad (1)$$
$$Cout = A.B + B.C + C.A \quad (2)$$

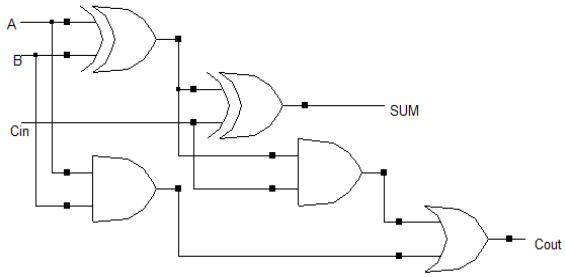

Figure1: Boolean circuit for Full adder

The Exclusive-OR and Exclusive-NOR gates are the basic components in designing of Full adder[3]. The performance of Full adder can be enhanced by improving the performance of XOR/XNORgates. The XOR/XNOR gates can be designed using basic logic gates i.e., AND, OR, and NOT gates. Efficient designing of these logic gates enhance the performance of Full adder cell thus increase the performance of a complete VLSI system since these gates are used as sub blocks in larger systems. XOR/XNOR cell implementation with minimum number of transistor is desirable in efficient VLSI system designing as it is area efficient and power efficient system [4-6].

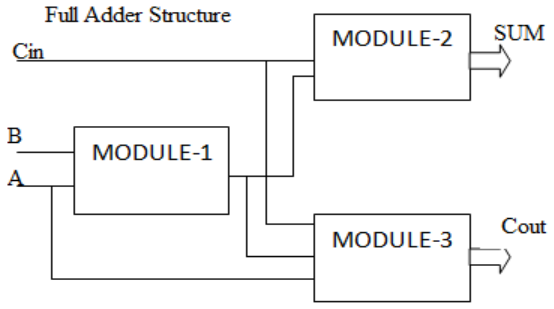

Figure2: Structure of Full Adder

Structured implementation diagram of 1-bit full adder using XOR/XNOR cell has been represented in figure2 [7, 8]. Module-1 is represented as XOR/XNOR gate,

which perform XOR or XNOR operation on inputs A and B. Module-2 is further represented as XOR/ XNOR gate, having inputs Cin and output of Module-1. The output of Module-2 is considered as SUM of full adder cell.Carry logic could be given by Module-3 which works as a 2:1 multiplexer, having inputs A, Cin and gives Cout (carry) as output [9-11].

II. FULL ADDERSCHEMATIC DESIGN

A. XOR/ XNOR cells and 2:1 MUX :

In this section the design approaches are mentioned for full adder cell using XOR/XNOR gates and 2:1 multiplexer. Figure 3 and Figure 4 represent the schematics of XOR and XNOR gates using 4-transistors respectively. Figure 5 is DSCH schematic of 2:1multiplexer which will be used to provide the carry logic in full adder design.

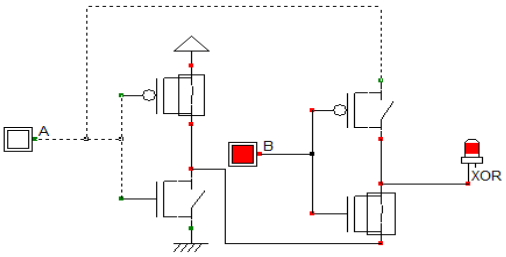

Figure 3: 4-Transistor XORcell

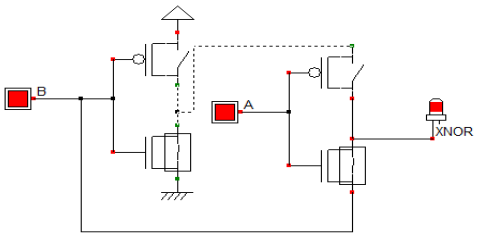

Figure 4: 4-Transistor XNOR cell

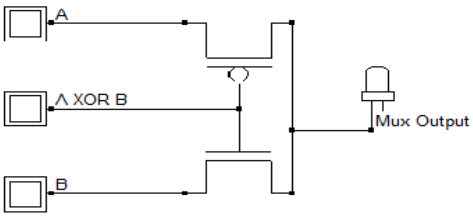

Figure 5: 2:1 Multiplexer

B. 10-Transistor Full Adder schematic in DSCH:

Figure 6 and Figure 7 represent the Full adder schematic design in DSCH software using XOR and XNOR cells and 2:1 mux respectively.

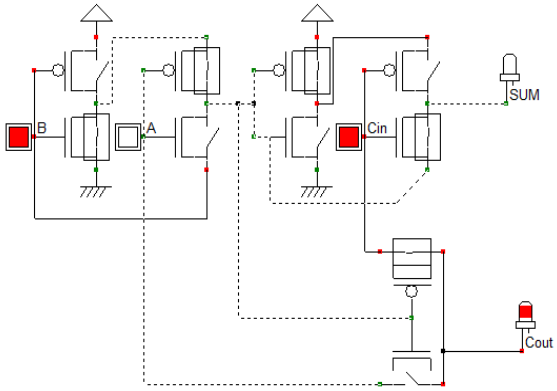

Figure 6: 10-T XNOR/Full Adder schematic

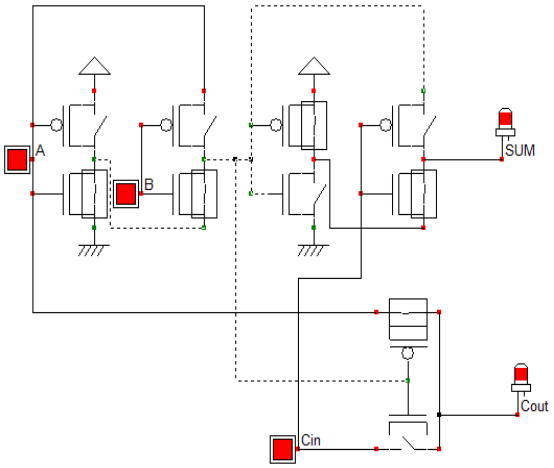

Figure 7: 10-T XOR/Full Adderschematic

III.LAYOUT DESIGN AND SIMULATION

In this paper two different approaches are adopted for layout designing. In first approach the auto generated layout has been obtained in µwind by compiling the Verilog file generated by DSCH and the second approach through which the layout is designed manually. The auto generated layout for XOR/ Full Adder and XNOR/Full Adder are shown in figure 8 and figure 9 respectively. Figure 10 and Figure 11 represent the manually generated layout for XNOR/ Full Adder and XOR/Full Adder respectively.

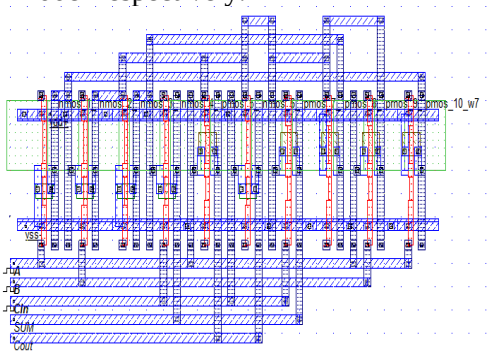

Figure 8: Auto generatedLayout forXOR/FA

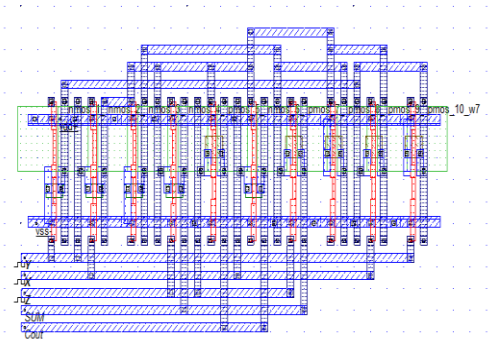

Figure 9: Auto generatedLayout for XNOR/FA

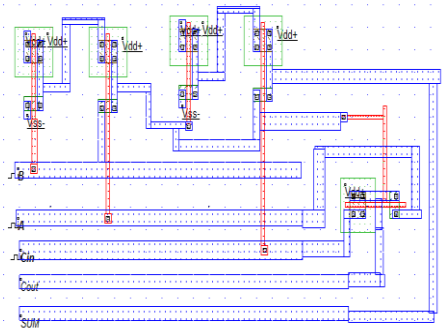

Figure 10: Semi Custom Layout for XNOR/FA

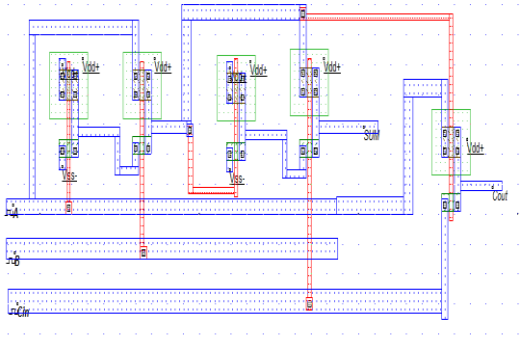

Figure 11: Semi Custom Layout for XOR/FA

Figure 12, 13, 14 and 15 show the simulated results obtained from µwind for auto generated layouts and self-generated layout for XOR/XNOR full adder circuit.

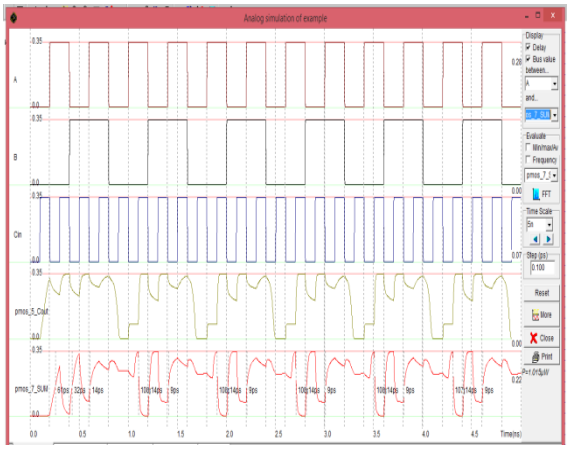

Figure 12: Analog simulation result for autogenerated XNOR/ FA.

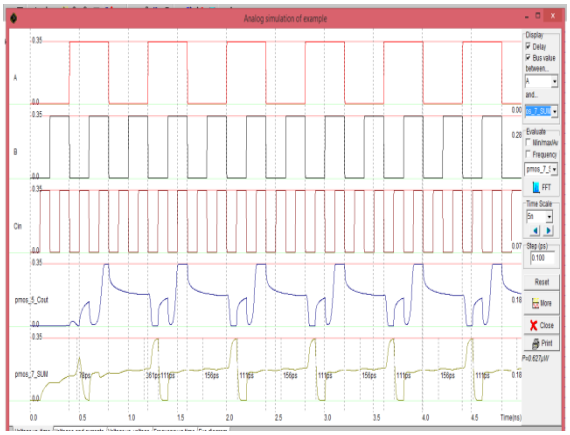

Figure 13: Analog simulation result for auto generated XOR/FA.

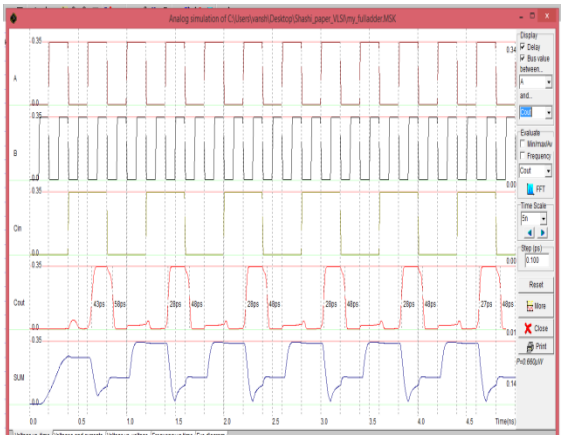

Figure 14: Analog simulation result forsemi-custom XNOR/ FA

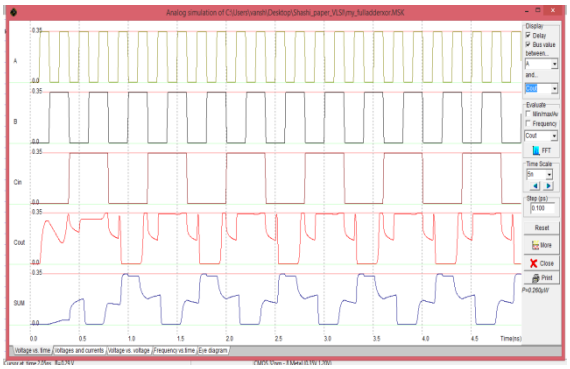

Figure 15: Analog simulation result for semi-custom XOR/FA

IV. COMPARATIVE ANALYSIS

In this paper power and area consumption for the auto generated layout and manually generated layout of XOR and XNOR based full adder cell has been compared. Table 1 is showing the comparison of different powers. From table 1 is clear that power consumption is less in manually designed layout as compared to auto

generated. Further, it has been clear that XOR/FA consumes less power as compared to XNOR/FA.

Table 1: Tabular comparison of Power consumption

Design	Power (microwatt)	
	XOR/FA	XNOR/FA
Auto generated layout	0.627 µW	1.015 µW
Semi-custom layout	0.260µW	0.660 µW

Table 2 is representing the comparison of consumed area for different layout design approaches. From the tabular comparison it is clear that manually designed layout for XOR/XNOR Full adder cell is area efficient than auto generated layout from DSCH.

Table 2: Tabular comparison of consumed area

Design	Area(in μm^2)	
	XOR/FA	XNOR/FA
Auto generated layout	27 μm^2	27 μm^2
Semi-customlayout	13.1 μm^2	15.1 μm^2

Graphical comparison of consumed power and area for auto generated layout and self-generated layout has been further shown by bar chart in Figure 14 and Figure 15 respectively.

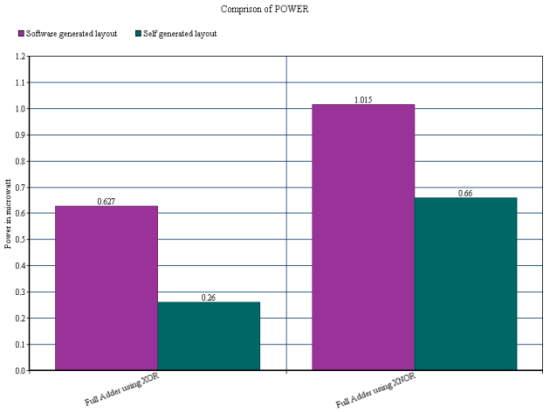

Figure 14: Graphical Comparison of Powers

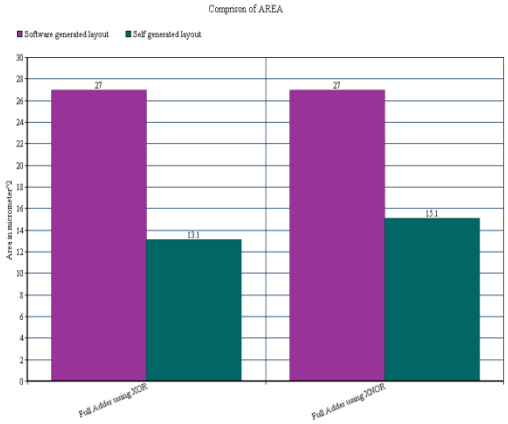

Figure 15: Graphical Comparison of Areas

V. CONCLUSION

In this paper two different approaches for layout designing: Auto generation through DSCH and semi-custom layout designing using µwind are discussed and compared for XOR/XNOR full adder cell using 32 nm CMOS technology. These comparisons were made interns of power and area. Simulated results in this paper show that semi customized design has better power efficiency and consumes less area as compared to auto generated layout. It means self-generated layout always show better performance in terms of power and area as compared to auto generated layout .

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References

1. R.UMA, VidyaVijayan, M. Mohanapriya, Sharon Paul, "Area, Delay and Power Comparison of AdderTopologies", International Journal of VLSI design & Communication Systems (VLSICS) Vol.3, No.1, February 2012, pp. 153-168.
2. Hanho Lee and Gerald Soblman, "A new low_voltage full adder circuit", IEEE International Symposium on Circuits and Systems, 1997, pp. 88-92.
3. Suman Nehra and P. K. Ghosh, "Design of a Low Power XNOR gate Using MTCMOS Technique", Advance in Electronic and Electric Engineering. ISSN 2231-1297, Vol. 3, Number 6 (2013), pp. 701-710.
4. Shivani Singh, Buddhi Prakash Sharma, Sanjay Singhal, "An Area Efficient Low Power TG Full Adder Design using CMOS Nano Technology", International Journal of Engineering Research &

Technology (IJERT), ISSN: 2278-0181, Vol. 3 Issue 4, April – 2014, pp. 2197-2201.
5. R. Shalem, E. John, L. K. John, "A Novel Low Power Energy Recovery Full Adder Cell", in Proc. IEEE Great Lakes VLSI Symp., Feb. 1999, pp. 380-383.
6. K.-H. Cheng and c.-S. Huang, "The novel efficient design of XOR/XNOR function for adder applications", in Proc. of the 6th IEEE International Conference on Electronics. Circuits and System, Vol. 1, 1999, pp.29-32.
7. B. Dillikumar, K. Charankumar , M. Bharathi, "Low power multiplexer based full adder using passtransistor logic", International Journal of Advanced Research in Computer Engineering & Technology Volume 1, Issue 5, July 2012, pp. 291-296.
8. Ahmed M. Shams and Magdy A, "A structured approach for designing low power adders," Conference Record of the Thirty- First Asilomar Conference on Signals, Systems & Computers, vol.1, Nov. 1997, pp.757-761.
9. S.Murugeswari, S.KajaMohideen, "Design of Area Efficient and Low Power Multipliers using Multiplexer based Full Adder", 2nd International Conference on Current Trends in Engineering and Technology, ICCTET'14, IEEE Conference Number – 33344, July 8, 2014, pp. 388-392.
10. Ranjeeta Verma, Rajesh Mehra , "CMOS Based Design Simulation Of Adder /Subtractor Using Different Foundriess", International Journal of Science and Engineering , Volume 2, Number 1 – 2013, PP:28-34.
11. Vandana Choudhary, Rajesh Mehra, "2- Bit Comparator Using Different Logic Style of Full Adder", International Journal of Soft Computing and Engineering (IJSCE)ISSN: 2231-2307,Volume-3, Issue-2, May 2013.

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