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DESIGN AND PERFORMANCE ANALYSIS OF AREA EFFICIENT CMOS DECODER CIRCUIT

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ABSTRACT
In recent years due to the magnificent development in CMOS technology to reduce area and power of chip designs take attention in research area. Decoder plays an important role in the code conversion and encryption of codes. It is having application in much area. A decoder is used to change a code into a set of signals and translate the encoded data in its original form. In this paper Decoder has been designed and simulated using different CMOS layouts. Design methodologies are used such as standard cell based design, semi custom design and full custom design of the Decoder to reduce area, power and size of the circuit. The paper analyzes and optimizes area and power of the Decoder using 90 nm technologies. The area gets reduced in full custom design by 50.57% from standard layout and 42.68% from semi custom design. The complexity and area get reduced in the full custom designed.

Key Words: *CMOS technology, Combinational circuits, IC layout, Very large scale integration.*

1. INTRODUCTION

Electronic devices are extensively used in many different fields and the size of these devices is gradually reduced. This is due to the integrated circuit technology. An integrated circuit or monolithic integrated circuit is a set of electronic circuits on one small plate called "chip" of semiconductor material, mostly silicon. Integrated circuits are used in virtually all electronic equipment today and have revolutionized the world of electronics. In the growth of integrated circuit towards the large integration density with high operating frequency the concern issues are power, delay and smaller silicon area with higher speed [1]. Computers, mobile phones, and other digital home appliances are now inextricable parts of the structure of modern societies, made possible by the low cost of integrated circuits. ICs have two main advantages over discrete circuits which is cost and performance. There is the technology which is used to construct integrated circuit which is CMOS technology. CMOS stands for Complementary Metal Oxide Silicon technology is recognized as the leading VLSI systems technology [2]. "CMOS" refers to both a particular style of digital circuitry design and the family of processes used to implement that circuitry on integrated circuits (chips). CMOS circuits use a combination of p-type and n-type metal–oxide–semiconductor field-effect transistors (MOSFETs) to implement logic gates and other digital circuits. For the most recent CMOS feature sizes, leakage power dissipation has become an overriding concern for VLSI circuit design [3]. CMOS technology comprising the pull up and pull down network where pull up network consist PMOS and pull down network consist NMOS circuit. CMOS is used in microprocessors, microcontrollers, static RAM, and other digital logic circuits.

Because of the combination of these thousands of CMOS transistors into a single plate to create a very large integrated circuit. VLSI stands for "Very Large Scale Integration" which includes packing more and more logic devices into smaller and smaller areas. Digital VLSI circuits are predominantly CMOS based. The huge chips that can be fabricated today are possible only because of the extremely low power consumption and smaller area of CMOS circuits [4].

2. DECODER

A decoder is a device which does the reverse operation of an encoder, decrypting the encoding so that the original information can be fetched. It is a combinational circuit that converts binary information from n input lines to a maximum of 2^n unique output lines. In digital electronics, a decoder can take the form of a multiple-input, multiple-output logic circuit that converts encrypted inputs into decrypted outputs, where the input and output codes are different. Enable inputs must be on for the decoder to function, otherwise its outputs assume a single "null" output code word. Logic design is guided by the requirements imposed on the implementation, such as performance and power [5]. Decoding is necessary in applications such as data multiplexing, 7 segment display and memory address

decoding. Decoder circuit would be an AND gate because the output of an AND gate is "High" (1) only when all its inputs are "High." Such output is called as "active High output". If instead of AND gate, the NAND gate is connected the output will be "Low" (0) only when all its inputs are "High". Such output is called as "active low output". A slightly more complex decoder would be the n-to-2^n type binary decoders. These types of decoders are combinational circuits that convert binary information from 'n' coded inputs to a maximum of 2^n unique outputs. We can have 2-to-4 decoder, 3-to-8 decoder or 4-to-16 decoder.

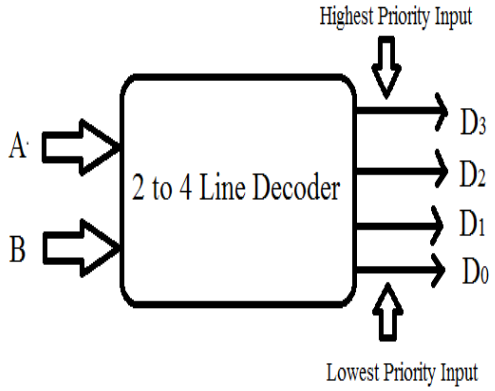

Fig. 1 Block Diagram of 2 bit Decoder

Fig. 1 Shows the Block diagram of 2 bit Decoder. In this diagram we have two inputs and four outputs. The output is decided according to the priority of inputs. The output which is the combination of low logic of inputs is set as lowest priority output and the output which is the combination of high logic of inputs is set as highest priority output. Decoder plays important role in the communication system [10].

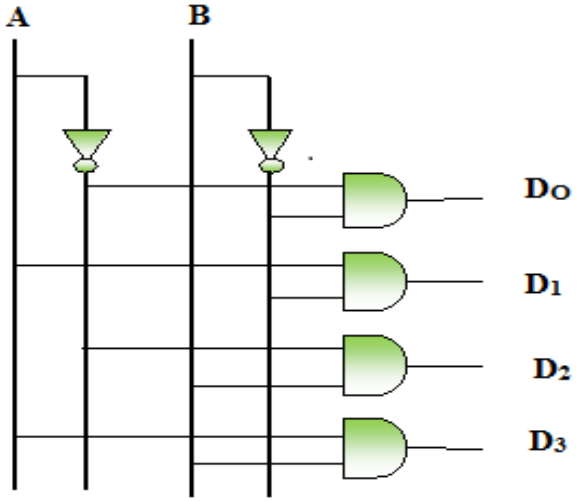

Fig. 2 Circuit Diagram of 2 bit Decoder

Fig.2 shows the circuit diagram of the decoder. In this diagram we realized the decoder expression using NOT gate and AND gate. The output is in term of the combination of the inputs. We have two inputs A and B and the outputs are D_0, D_1, D_2, and D_3. The Expression for the outputs is given as under:

$$D_0 = A'B' \quad (1)$$
$$D_1 = A'B \quad (2)$$
$$D_2 = AB' \quad (3)$$
$$D_3 = AB \quad (4)$$

Table.1 Truth Table of 2 bit Decoder

INPUT		OU.TPUT		
A	**B**	D_0 D_3	D_1	D_2
0	**0**	**1** 0	0	0
0	**1**	0 0	**1**	0
1	**0**	0 0	0	**1**
1	**1**	0 **1**	0	0

Table.1 Shows the Truth table of Decoder. In this table, according to the inputs the output is shown. The output D_0 is high when both the input is low. The outputs D_1 and D_2 are high when one of the inputs is low. The output D_3 is high when both the input is high.

3. SIMULATION AND RESULTS

Design processes are aided by simple concepts such as stick and symbolic diagrams but the key element is the design rules. Design rules are used to produce the workable mask layouts from which the various layers in silicon will be formed or patterned [6]. Complementary metal–oxide–semiconductor (CMOS) technology is being used in various digital and analog logic circuits such as image sensors (CMOS sensor), data converter circuits and decoding circuits [7]. The Schematic Diagram of 2:4 Decoders is given in Fig. 3. This diagram constructed by using two inverters and four AND gate. The input is in the form of switch and the

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corresponding output is shown by glowing of LED connected at the outputs.

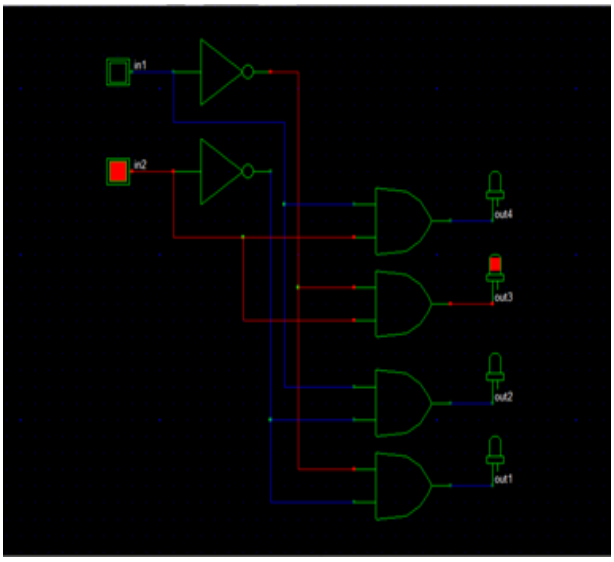

Fig. 3 Schematic Diagram of 2 bit Decoder

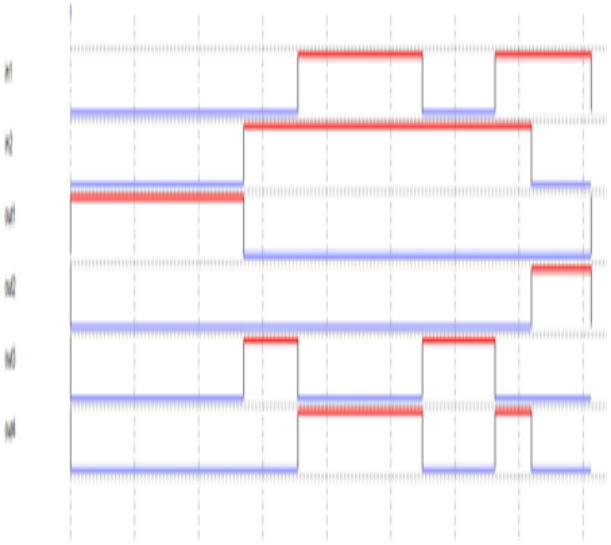

Fig. 4 Simulation Result of Schematic of 2 bit Decoder

Fig. 4 shows the simulated result of the Schematic diagram of the 2 bit decoder. In Fig. we have two inputs and four outputs. The inputs are in the form of two clocks and the output is varying according to the input clocks.

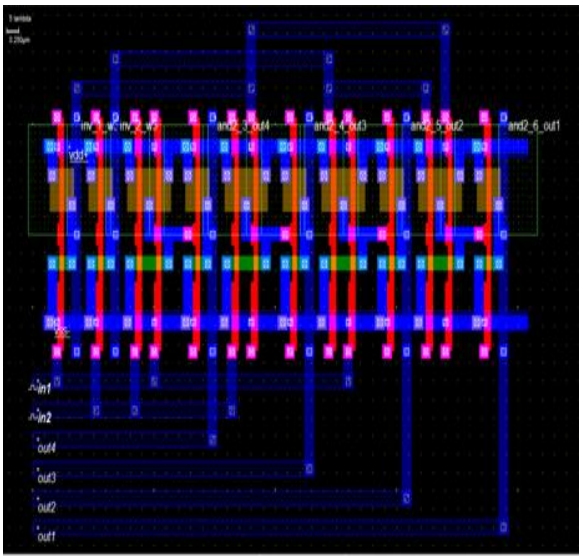

Fig. 5 Standard layout of 2 bit Decoder

Fig. 5 shows auto generated Standard layout of 2 bit Decoder. In this layout we have pull up and pull down network having CMOS technology. This Standard layout is very complex and consumes more area. Fig. 6 shows the corresponding simulated result of Standard Layout.

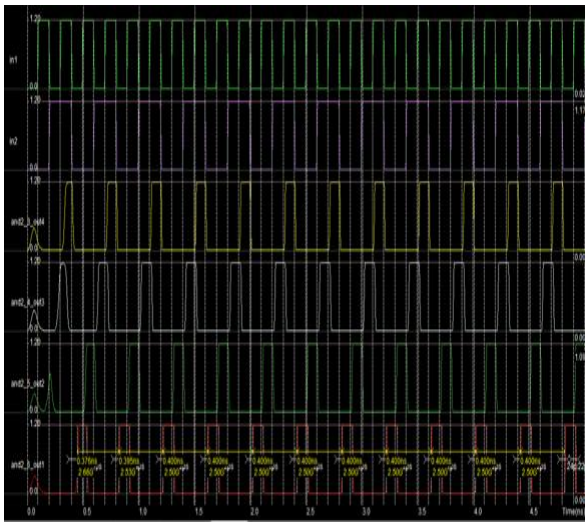

Fig. 6 Simulation Result of Standard Layout

Fig. 7 shows semi custom layout of 2 bit Decoder. In this layout we take PMOS and NMOS which already exists in library of the software. By using these PMOS and NMOS circuit we design the logic gates by self. In decoder two inverter and four and gate are needed. So we design AND gate with the help of self design NAND gate and inverter. The inverters are constructed in form of pull up and pull down network using PMOS and NMOS. This semi custom design is less complex using less area and power. Fig. 8 shows the corresponding simulated waveform of Semi custom Layout.

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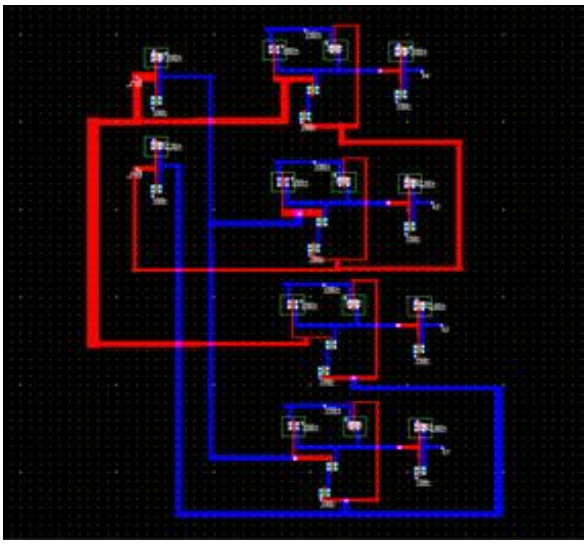

Fig. 7 Semi custom layout of 2 bit Decoder

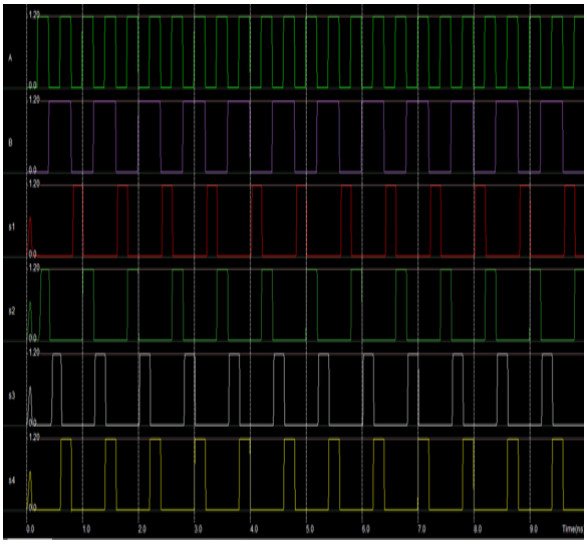

Fig. 8 Simulation waveform of Semi custom layout

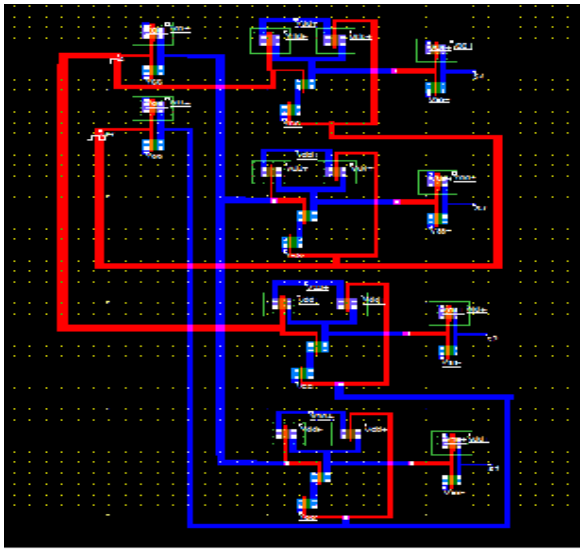

Fig. 9 Full custom layout of 2 bit Decoder

Fig. 9 shows full custom layout of 2 bit Decoder. In this layout we make PMOS and NMOS by itself using the diffusion element, metal, polysilicon, and well existing in the library. By using these PMOS and NMOS circuit we design the logic gates by self. In decoder two inverter and four and gate are needed. So we design AND gate with the help of self design NAND gate and inverter. The inverters are constructed in form of pull up and pull down network using PMOS and NMOS. This design is less complex and using less area in the layout but delay is more [8]. Fig.10 shows the corresponding simulated waveform of full custom Layout.

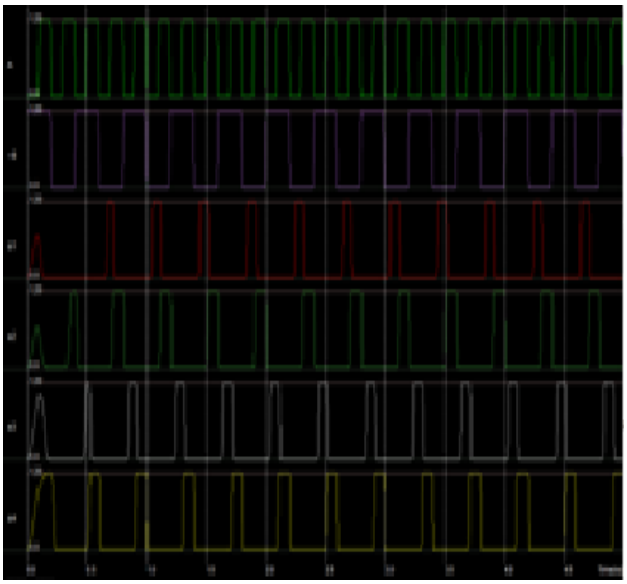

Fig. 10 Simulation waveform of full custom layout

4. COMPARITIVE ANALYSIS

In this paper the decoder is designed by the three different layout using CMOS technology. The three decoder layouts are the standard cell based design layout, semi custom based design layout and full custom based design layout.

The main parameters of consideration for analysis are area, complexity and power of the 2 bit Decoder design in this paper. Table 2 show the area and power consumption of 2 bit design using CMOS technology. Fig. 11 and Fig. 12 show the comparative analysis of power and area of different layout respectively.

Table 2 Area and Power consideration

DECODER LAYOUTS	TECHNOLOGY USED	AREA	POWER
Standard cell based design	90 nm	700.4 um^2	99.19 µW
Semi custom based design	90 nm	604.2 um^2	81.57 µW
Full Custom Design	90 nm	346.3 um^2	99.87 µW

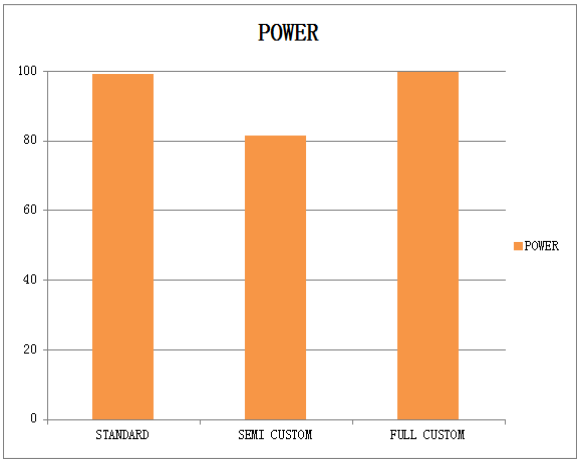

Fig.11 Power of different layout 2 bit Decoder

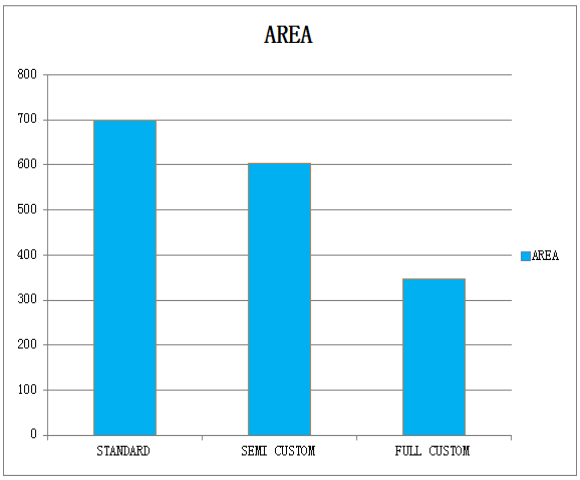

Fig.12 Area of different layout 2 bit Decoder

5. CONCLUSION

Today's integrated circuits have a growing need for speed, area, and power. Despite many advantages, CMOS suffers from increased area, more power dissipation and correspondingly increased capacitance and delay, as the logic gates become more complex [9].So we have to develop and simulate the those layouts which consume less area and power. It has been demonstrated from the simulated results of different layout that the area is reduced in the full custom design of the decoder circuit from standard cell layout and the semi custom based layout of the decoder. The power is reduced in the semi custom design from standard cell layout but increased in the full custom design. So reduction of power in the full custom design is the future aspect.

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