International Journal of Scientific Research Engineering & Technology (IJSRET) ISSN: 2278–0882
EATHD-2015 Conference Proceeding, 14-15 March, 2015

Layout Design and Simulation of CMOS Multiplexer

Priti Gupta
Electronics & Communication department
National Institute of Teacher's Training and Research
Chandigarh

Rajesh Mehra
Electronics & Communication department
National Institute of Teacher's Training and Research
Chandigarh

ABSTRACT
Multiplexer circuit is important device that have application in many field of Engineering. The research area of VLSI is to reduce area and complexity of the design. The purpose of this paper is to design 2 to 1 multiplexer with the help of CMOS logic to reduce area and complexity of the circuit. The different design methodologies are adopted in this paper to reduce the size, area and complexity of the multiplexer. This work evaluates 45nm technology. At the end, design methodologies are analyzed and optimize area of multiplexer is purposed.

Keyword- *Moore's Law, CMOS technology, Bipolar Transistor, Microwind tool, Layout*

1. INTRODUCTION

Very-large-scale integration (VLSI) is the technology of designing of an integrated circuit (IC) by combining thousands of transistors into a single chip. It is the design of extremely small, complex circuitry with the help of semiconductor material. It may contain millions of transistors on a single chip is known as Integrated circuit (IC). VLSI technology is based on Moore's law. According to the Moore's law number of transistors in a dense integrated circuit doubles approximately every eighteen months as shown in fig.1 [1].

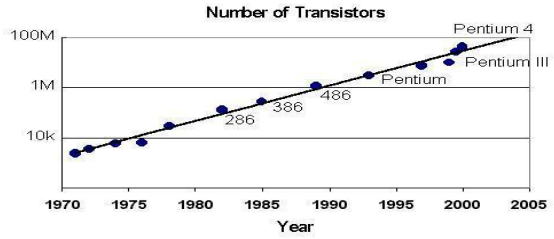

Fig. 1 Moore's Law

VLSI fabrication technology is still in the process of evolution which is leading to smaller line widths and features size and to higher density of circuitry on a chip. Scaling down of the feature size generally leads to improved performance. Micro electronics technology may be characterized in terms of several figure of merit [1].

1. Minimum feature size
2. Number of Gates on one chip
3. Power dissipation
4. Maximum operating frequency
5. Die Size
6. Production Cost

Figure of merit can be improved by changing the dimension of the transistor, separation between features and by adjusting the doping level and supply voltages. The design efforts have focused on optimizing speed to realize computationally intensive real-time functions such as video compression, gaming, graphics etc. There are different types of technology advancement in the VLSI design such as 90nm, 65mn, 45 nm etc. These technologies are used to improve the performance of the circuit in terms of the power, area, delay etc. These technologies depend on the distance between source and drain.

Multiplexer means many into one. Multiplexer is a device which selects one out of many inputs on the called control lines. A multiplexer is a circuit that is used to select and route any one of the several input signals to a single output. Fig. 2 shows the general idea of a multiplexer with 2^n input signal, n control signals and one output signal. A simple example of a non electronic circuit of a multiplexer is a single pole multi position switch. Multiplexer is used to perform high speed switching are constructed of electronic components.

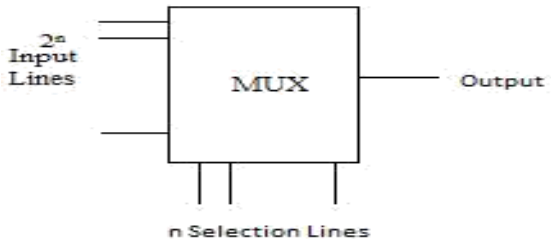

Fig.2 Multiplexer Concept

A 2 to 1 multiplexer is shown in Fig. 3 It has two inputs Io and I1, one selection line S and one output Y. The output of the 2 to I multiplexer is

$$Y=S'Io+ SI1 \quad (1)$$

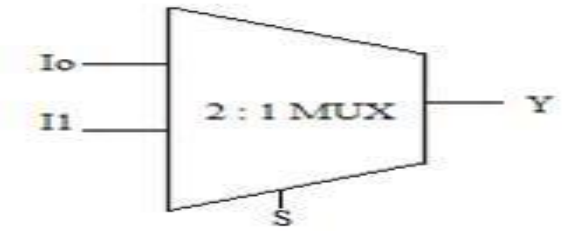

Fig. 3 2 to 1 multiplexer

The 2 to 1 multiplexer can be implemented with the help of NAND universal gate as shown in fig. 4

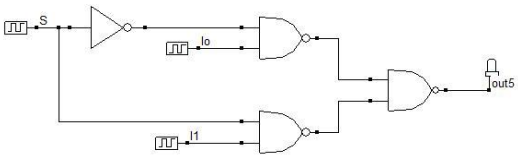

Fig. 4 Multiplexer using NAND Gate

The working truth table of multiplexer is as shown table 1 [4].

A	B	Output (Y0)
1	X	A
0	X	A
X	1	B
X	0	B

Table 1 Multiplexer output [4]

Multiplexer can work on analog as well as digital data. Multiplexer are built of relays and transistor switches for analog application but for digital applications, they are built from standard logic gates. The multiplexer is used for digital applications, also called digital multiplexer, is a circuit with many input but only one output. By applying control signals, we can steer any input to the output.

Multiplexers and de-multiplexers are common building blocks of data paths and are used extensively in numerous applications including processor buses, network switches and digital signal processing stages incorporating resource sharing [5]. Multiplexer designed for biomedical applications are low power consumption low on resistance and faithful reproduction of input at the output [6]. Multiplexer are used in various fields where multiple data need to be transmitted using a single line. Following are some of the applications of multiplexers –

1. **Communication System-** Communication Process is the process of transmitting information of the dedicated channel, which is received at the receiver side and such type of system is called communication system. The efficiency of communication system can be increased with the help of multiplexer. Multiplexer is used in the communication system to transmit different type of information, such as audio or video at the same time on a single transmission line.

2. **Telephone network -** Multiplexer is widely used in the telephone network to multiplex various audio signals on single line. In this way multiple audio signals can reach to the dedicated recipients with the help of multiplexer.

3. **Computer memory** – Another application of the multiplexer is to implement computer memory. It also reduces the number of copper wire to connect the memory with other computer parts.

4. **Transmission from the computer system of a satellite –** Multiplexer can be used in the satellite communication. It is used to transmit data from satellite or spacecraft to the ground system with the of help of GPS (Global Positioning System).

The latest technology used for constructing integrated circuits is complementary metal-oxide semiconductor (CMOS) [7]. A static CMOS gate is a combination of two networks, called the pull-up network (PUN) and the pull- down network (PDN). The function of pull up network is drive the Vdd towards output and function of the pull down network is drive output to supply Vss. The noise margin of the static CMOS logic is high [4].

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CMOS circuit requires very less power [8]. CMOS technology is widely used I the designing of the VLSI circuits T he static CMOS circuit is shown in Fig. 5

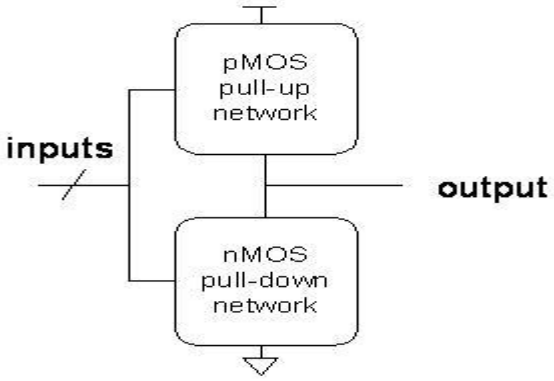

Fig. 5 Static CMOS Circuit

3. PROPOSED MULTIPLEXER USING CMOS

There are two types of MOS, i.e. the NMOS and the PMOS. Where NMOS transistor can gives the "LOW" signal completely, but it has poor performance at "HIGH" signal. Same as in PMOS transistor which gives the "LOW" signal completely but poor performance at "HIGH" signal [3][9]. CMOS transistor is the combination of NMOS and PMOS transistor which gives full output voltage swing. Power consumption is very less in CMOS circuits compared to the NMOS design and bipolar transistors. There are different design methodologies of designing of integrated circuit such as full custom design, semi custom design and standard cell based design. In standard cell design, a design is captured using the standard cells available in a library via schematic or HDL [2]. In the full custom design the function and layout of practically every transistor is optimized [2]. This paper is based on the area efficient design 2 to 1 multiplexer using microwind tool.

The schematic diagram of 2:1 MUX is as shown in fig.6. This circuit is designed with the help of universal NAND gates where 7 PMOS and 7 NMOS are used. The total numbers of 14 transistors are used in the CMOS design. P Switch is connected to the V_{dd} to the output and N switch is connected to the output to V_{ss} [2]. In this CMOS design NMOS works as pull down network and PMOS works as pull up network.

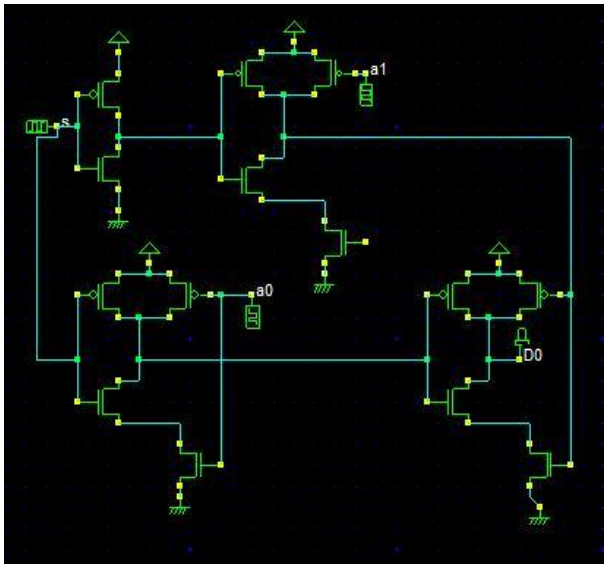

Fig. 6 Schematic of 2 to 1 multiplexer using NAND gates

Fig.7 shows the standard cell multiplexer layout design. Standard cell multiplexer design is complex and consumes more area.

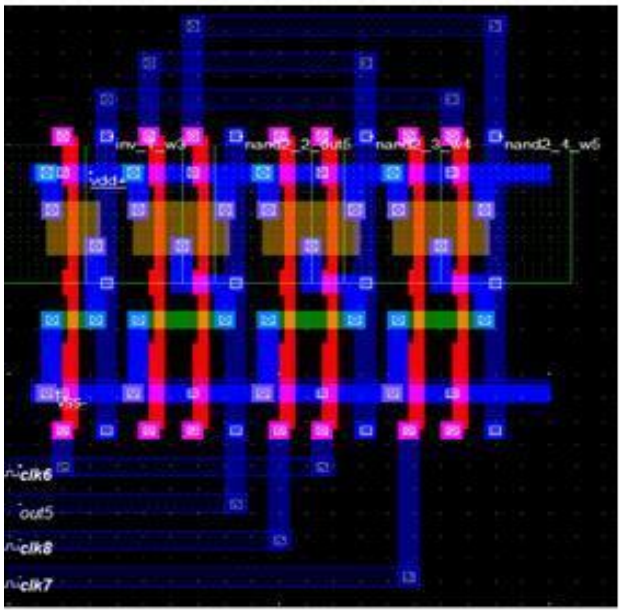

Fig.7 standard cell layout Design of 2 to 1 Multiplexer

Another layout design of the 2 to 1 multiplexer has created based on semi custom design method is shown in fig. 8. Common supply is given to the all the transistor to reduce the power consumption in the 2 to 1 multiplexer circuit. Here combined n well is used in NAND gate to reduced power consumption and complexity in the semi custom layout design in comparison to standard cell

based layout design.

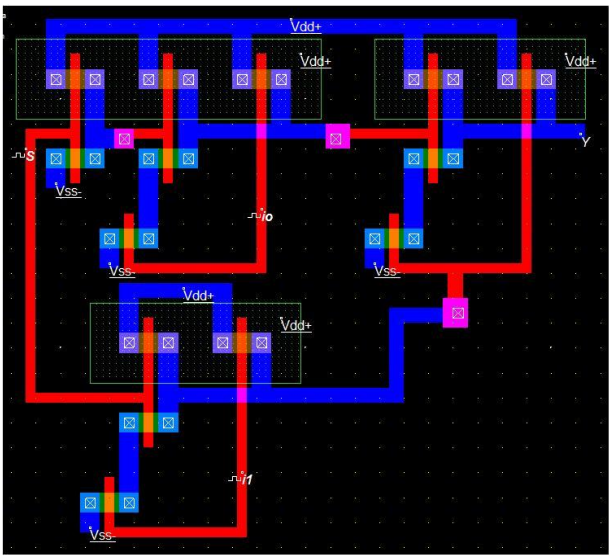

Fig. 8 Semi Custom Design of 2 to 1 Multiplexer

Fig. 9 shows the design of 2 to 1 multiplexer using full custom layout design. Here all the PMOS's has designed with common n well. Common n well requires single supply to the circuit and reduces the power consumption in the 2 to 1 multiplexer circuit.

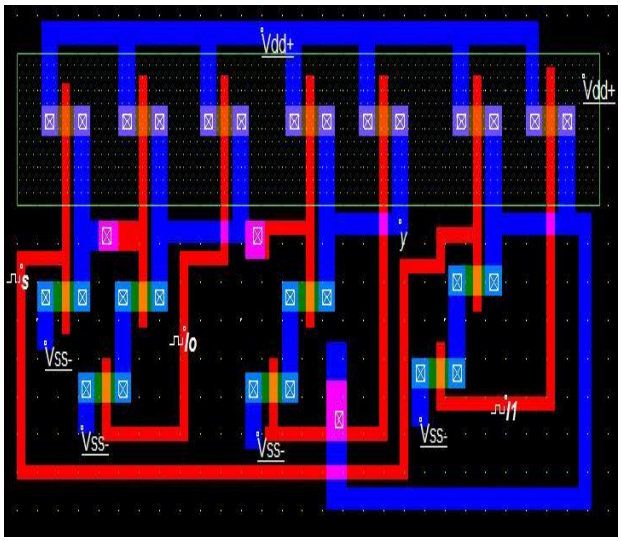

Fig. 9 Full Custom Design of 2 to 1Multiplexer

Fig.10 shows the simulation waveform of 2 to 1 multiplexer circuit. Here S is the selection line, Io and I1 are inputs and Y is the output. When S is low, output will follow I0 i.e. Y=I0. When S is High, output will follow the I1 i.e. Y=I1. In this way the logic has been verified for standard based design, semi custom design and full custom design.

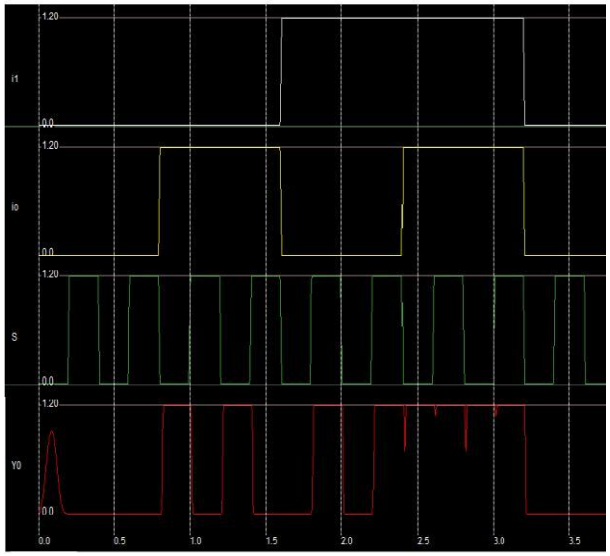

Fig. 10 Simulation Result of 2 to 1 Multiplexer

4. COMPARATIVE ANALYSIS

The main parameters of consideration are area, complexity and power of the 2 to 1 multiplexer in this paper. Table 2 shows the area and power consumption of 2 to 1 multiplexer circuit.

Multiplexer Layout	Technology Used	AREA Used	POWER Consumption
Standard Cell based Design	45nm	8.2 μm^2	8 nW
Semi-Custom Design	45nm	7.5 μm^2	0.384 µW
Full Custom Design	45nm	5.8 μm^2	0.247 µW

Table 2 Area and Power consideration

Here 45nm technology is used in the designing of standard cell based layout, semi custom based layout and full custom layout of 2 to 1 multiplexer with the help of microwind tool. Transistor width (w) = 0.200 micrometer and length L=0.100 micrometer has been used in the design.

5. CONCLUSION

This analysis has proposed three different type layout design of 2 to 1 multiplexer. Standard cell based layout, semicustom based layout and full custom layout are developed for the 2 to 1 multiplexer. Area, power and complexity of the different design methods are the parameters taken for analysis. Fig. 11 shows that semi custom based layout design has 8.53% of reduction in the area compared to the standard cell based design. Full custom design has 29.26 % of reduction in the area compared with the standard cell and 22.66 % reduction in the area compared than semicustom based design layout. In terms of complexity, Semi custom based layout and full custom layout is less complex than standard cell layout. Power consumption of the full custom layout design is 35.67 % less than semicustom based layout design.

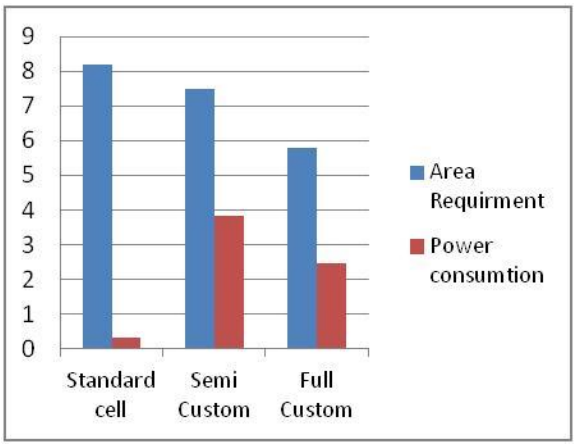

Fig.11 Area and Power consideration of different type cell

Acknowledgement

Authors would like to thank, Director, National Institute of Teacher Training and Research, Chandigarh and Director Kashi Institute of Technology, Varanasi for their inspiration, motivation and support throughout this research.

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