

Design of Low Power High Performance JK Flip Flop

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Abstract - This paper presents the design of low power, high performance JK flip flop. The rapid technical trends are emerging to decrease the geometrical feature size and power consumption of VLSI designs. The proposed design shows the comparison between auto generated and semicustom layout of JK flip flop. The proposed flip flop can save up to 32% of the power and 50% of area. Therefore proposed design is more optimized than the auto generated because the efforts have done to use the minimum area during layout designing.

Keywords: VLSI design, JK flip-flop, CMOS technology, power

1. INTRODUCTION

In this paper DSCH3.1 is used as a logic editor and simulator .DSCH3.1 is used to verify the architecture of the logic circuit. It provides a user friendly interface for further logic design, simulation and analysis [1]. The MICROWIND allows to work on the layout partof the circuit and gives the analysis of power consumption and other parameters on pressing a single key along with Design Rule Check (DRC).In recent years, with the increase in the frequency of clock and complexity in high performance VLSI chips, the increase in the power consumption has become the major obstacle in the realization of performance designs [2]. Power consumption has attracted more concern of manufacturer on VLSI circuit design. A flip flop is a circuit that has two stable states and can be used to store information. A flip flop can be defined in the term as a bitable multivibrator. When it is used in finite state machine, the output and next state depend not only on its current input, also on its current input State [3]. It is basically used as a memory element. It can also be used for counting of pulses, and for synchronizing variably timed input signals to some reference timing signals. A JK flip flop covers the characteristics of an RS, a T, and a D flip flop, and is widely applied in digital systems [4]. But circuit configurations of JK flip flops are more complex and their power dissipations are higher. Than those of other types of flip flops. The circuit complexity and high power

dissipations of JK flip-flops limit their implementation in a large scale integration [5].

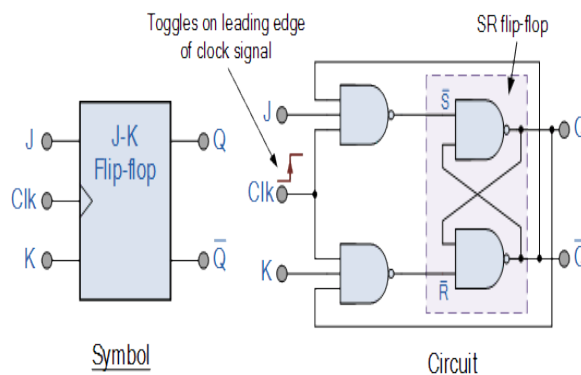


Fig.1 JK flip flop using NAND gates

2. JK FLIP FLOP

Flip-flops are crucial and vital component where the output at any instant of time depends on the past output and present input. Hence, flip-flops are also known as a memory element. These memory elements composes of NOT, OR, AND, NOR, NAND, CMOS latches [6, 2]. A JK flip-flop is used in sequential circuits and can be used as data processors [7]. Most of the appliances operate on the battery, so that the power dissipation becomes one of the major constraints [8].

Table. 1 Truth table of JK flip flop

J	K	CLK	Q
0	0	↑	Q ₀ (no change)
1	0	↑	1
0	1	↑	0
1	1	↑	\bar{Q}_0 (toggles)

JK flip-flop was invented by Jack Kilby that is why the name given to the inputs of the flip-flop is J & K. This flip-flop is also called a gated S & R flip-flop with the addition of a clock input circuitary which discards the invalid output condition occurring when both inputs S & R are equal to logic level '1' [9]. By addition of this clocked

input, JK flip-flops have four possible input combinations viz. 'logic 1', 'logic 0', 'no change' & 'toggle'[10].

Table 2. Excitation table of JK flip-flop

Q	Q _{next}	Comment	J	K
0	0	no change	0	×
0	1	Set	1	×
1	0	Reset	×	1
1	1	Toggle	×	0

The combination of J=0 & K=0 gives the command to stay in the hold state [11]. Similarly when J=1 & k=0, gives the command to set the flip-flop, when J=0 & k=1, it resets the flip-flop & the last combination i.e. when J=1 & K=1, is the command in which flip-flop toggles [12, 1]. This is to be avoided during the ideal working.

The characteristic equation of a JK flip-flop can be written as:

$$Q_{next} = J\bar{Q} + \bar{K}Q \dots\dots\dots(1)$$

In this paper CMOS technology is used for designing the JK flip-flop. Flip-flop is NAND based and gates are constructed by using p-Mos & n-Mos.

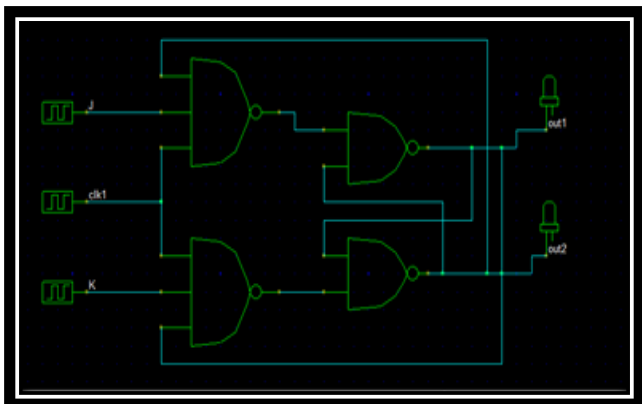


Fig.2 Schematic of JK flip-flop

Combined clock is given to the 3 input two NAND gates, along with input J & K. by means of which power consumption get reduced.

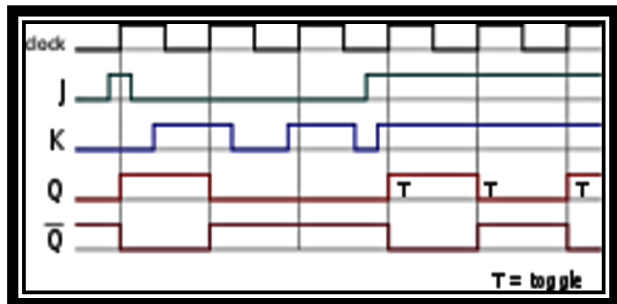


Fig.3 Transient waveform of JK flip-flop

3. PROPOSED JK FLIP-FLOP USING CMOS

This propounded circuit is designed by using strong 1 (pull up) and strong 0 (pull down) transistors namely P - MOS and N -MOS transistors.

In the below figure, two 3 input NAND gates and two 2 input NAND gates have been used.

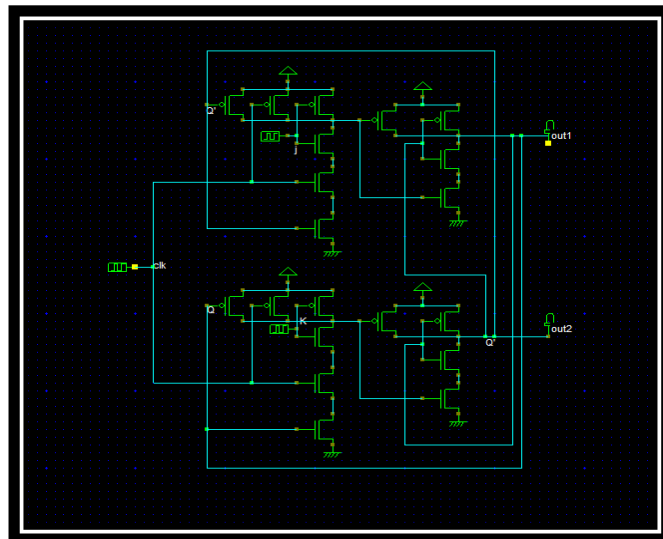


Fig.4 Schematic JK flip flop in DSCH31

Wherease out of them 10, n-mos transistors and 10 p-mos transistors, having total of 20 transistors. The efforts are done to give the common V_{dd} supply to reduce the power consumption.

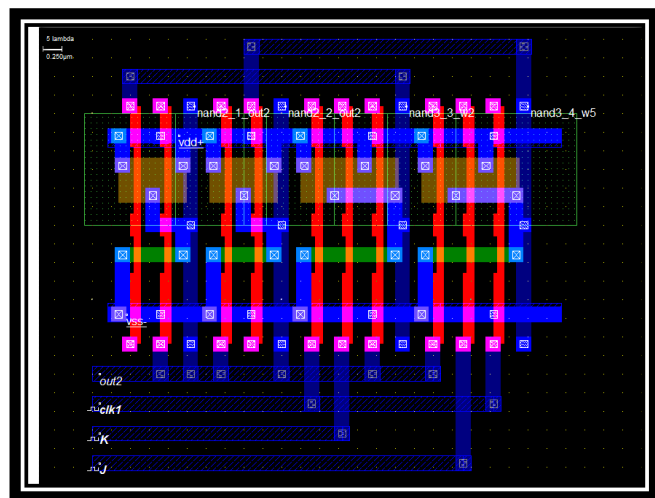


Fig.5 Autogenerated layout of JK flip flop

These waveforms correlate with the working of the JK flip flop.

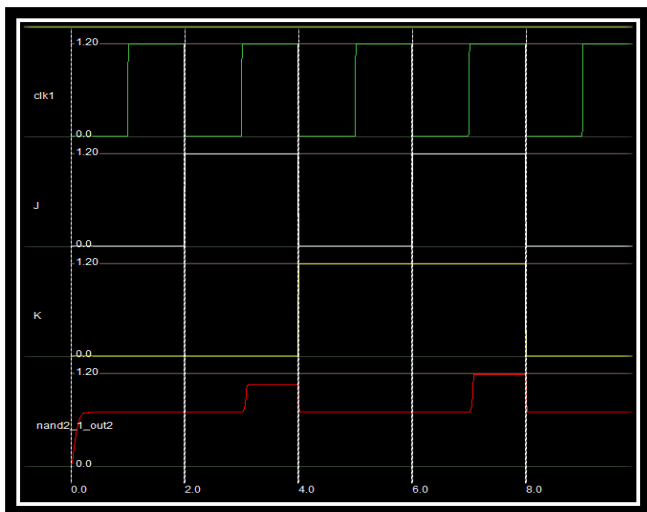


Fig.6 Simulated waveforms

The semicustom layout has been generated by using the inbuilt n-mos and p-mos with self-generated metal & polysilicon connections. This design will lead to the less area consumption & low power consumption.

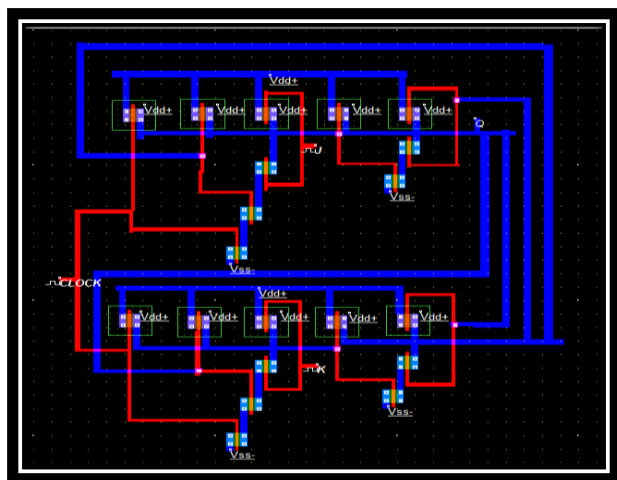


Fig.7 Semicustom layout of JK flip-flop

4. SIMULATION & ANALYSIS

The below table is drawn on the basis of two parameters viz. power consumption & area used. Here analysis has been done using the layout technique i.e. autogenerated and semicustom. Secondly the design nm technologies, 180nm, 90nm, 65nm.

Table 2 for power and area analysis

Parameter considered	Technique used	Auto generated Layout	Semi Custom layout
Power used	90 nm	9.815 μ W	7.436 μ W
	65 nm	0.619 μ W	0.469 μ W
	45 nm	0.511 μ W	0.387 μ W

Area used	90 nm	37.7 μ m ²	42.2 μ m ²
	65 nm	18.5 μ m ²	20.6 μ m ²
	45 nm	9.4 μ m ²	10.5 μ m ²

5. CONCLUSION

The proposed analysis method provides the track of low power consumption by self-designing the layout part of the circuit. From above table we can conclude that, the power consumption in autogenerated is more in comparison to semicustom design and nearly 1000 times. On changing the technology from 90 nm to 65 nm and 65 nm to 45nm, the power consumption also reduces. But there is a large reduction in power consumption from 90nm to 65nm and a little bit reduction in power consumption from 65 nm to 45nm. When we move from 90 to 65 to 45 the area is reduced by 50% in both the autogenerated and semicustom layout.

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