ACTIVE-PASSIVE DELTA SIGMA MODULATOR FOR LOW POWER APPLICATIONS

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Abstract

This paper proposes the design of active-passive delta-sigma modulator using low gain amplifier and switched capacitor network to enable SC integrator function. Compared with the conventional op-amp based SC integrator this design is intended to minimize power consumption. Since open loop amplifier requires low dc gain and implements built in current adder, the power consumption is low. Delta-sigma modulator is designed using standard 180nm technology suitable for low power applications.

Keywords: *Delta-sigma modulator, low-gain amplifier-based switched-capacitor (SC) integrator, passive SC integrator.*

I. INTRODUCTION

The increasing demand for portable electronics such as personal wireless communication devices, digital cameras, personal audio devices used in daily life continues to drive the need for highly power efficient data converters with high resolution. Powered by batteries, their supply voltage is often limited, and the battery lifetime is of great importance for these devices. All these factors address the requirements of low-voltage low-power system building blocks. Delta-sigma modulators are the preferred solution and the ones based on switched capacitor (SC) are optimal for low power medium conversion speed because of their accurate setting of zeros of the noise transfer function (NTF) and their insensitivity toward clock jitter [1].As is known, delta-sigma modulator demands using one operational amplifier (op-amp) per zero of the NTF and this results in relatively high power consumption, which becomes a limitation in many applications [2], [3].Sharing the op-amp [4] and special techniques [5]-[7] reduces the number of active blocks but performance will be poor. Even the use of a passive modulator [8]-[12], consisting of switches, capacitors, and quantize only, reduces the power. However, the passive operation causes a loss in the NTF that reduces the signal along the architectures, thus reduces the signal-to-noise ratio(SNR) and attenuates the signal along the architecture, thus making the thermal noise dominant[10].To overcome the reduced loop gain problem in the passive delta-sigma modulator, several active-passive hybrid implementations were presents[13]-[15].A fourth-order continuous-time(CT) active-passive modulator employs two amplifiers with passive networks to achieve a high SNR. The active stage utilizes a fully functional op-amp which has stringent requirements and leads to a high power consumption[13].A fifth-order CT hybrid active-passive modulator which uses three high power active integrators and two passive integrators, and which also employs a low-gain preamplifier with a dynamic comparator, can only obtain a 10-bit resolution[14].A third order discrete time(DT) active-passive modulator employs a power hungry Gm-C integrator in the second stage and passive integrator in the first and third stages; besides, it also uses preamplifier in front of the comparator. Because of the inability to define an accurate NTF zeros from the passive integrators and the thermal noise limit delta-sigma modulator to 9-b resolution [15].

None of the above active –passive modulators presented in the literature improves the traditional passive SC integrator structure for better noise shaping in the delta-sigma modulator.

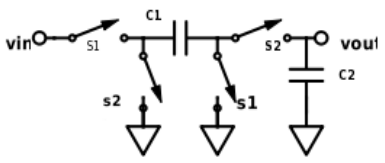


Fig 1.Passive SC integrator

This paper presents hybrid solutions that use active functions to compensate for the limits of passive operation. It uses three techniques for decreasing power consumption. The main one consists of using a forward gain k and a positive feedback across a passive SC integrator. The method needs a gain stage though. Second, its required low gain is obtained with a circuit that embeds the positive feedback. Since the amplifier includes a built in adding function for superposing the signal and the feedback path, the power required is very low. Third, power reduction for a single bit modulator is proposed with feed-forward and built-in adder to assist the first amplifier. This improves the linearity and relaxes the slew rate requirements are relaxes; the resulting power consumption is very competitive.

The technology used is a 180-nm CMOS. After the introduction, Section II describes the integrator with a low gain amplifier. Section III describes the system-level architecture for high order active-passive delta-sigma modulator. Section IV describes the circuit level implementation of SC integrator. Section V provides simulation results. Section VI summarizes the paper's conclusions.

II. INTEGRATOR WITH LOW GAIN AMPLIFIER

The integrator grants the lowest consumed power is the passive SC implementation shown in fig.1.But the transfer function is not one of the ideal integrators $H1=z^{-1}/(1-z^{-1})$ used in delta-sigma modulator. The transfer $Hp= \alpha z^{-1}/ [1-(1-\alpha) z^{-1}]$ (α=C1/ (C1+C2) implies a gain error and a phase error. The gain error is more important than phase error because it causes signal attenuation and this give rise to a more critical noise performance. Phase error also problematic because it describes the shift of the integrator pole inside the unity circle.

$$\frac{Vout}{Vin}=H(z)=\frac{k\alpha z^{-1}}{[1-z^{-1}+\alpha(1-\beta)z^{-1}]} \text{----- (1)}$$

Positive feedback around SC integrator can compensate for the phase error and forward gain can compensate gain error. β=1 makes the integrator transfer function ideal in terms of elimination of phase error. However, since $\beta>1$ would bring the pole into the region of instability. The circuit realizing the forward gain and feedback branch consumes power.

The parallel connection of two differential pairs with resistive load can achieve the result. The currents and the aspect ratio of transistors determine the value of β and K. The gains of branches of the circuit Fig 2(b) are K=gmK RL and β=gm β RL, where gmK , gm β are the trans-conductance's of the two differential pairs. The value of K is not critical but the value of β must be equal to 1 in order to achieve the required compensation.

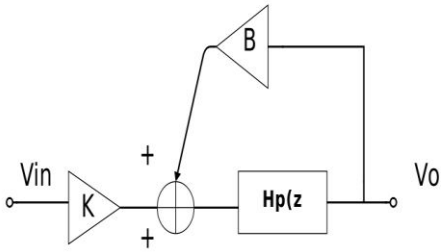


Fig2. (a)Compensation technique model

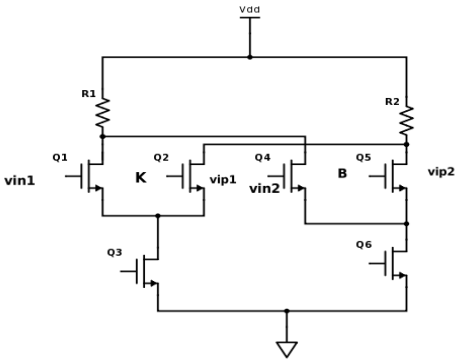


Fig 2. (b) Circuit implementation.

III. ACTIVE-PASSIVE INTEGRATOR IN A HIGH ORDER ΔΣ MODULATOR.

An active-passive integrator that replaces a conventional integrator in delta-sigma architecture greatly reduced consumed power.

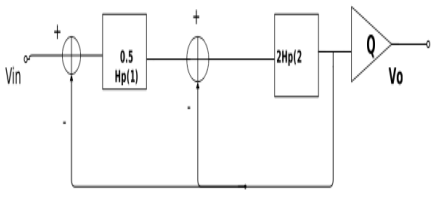


Fig3. (a)Second order delta-sigma modulator

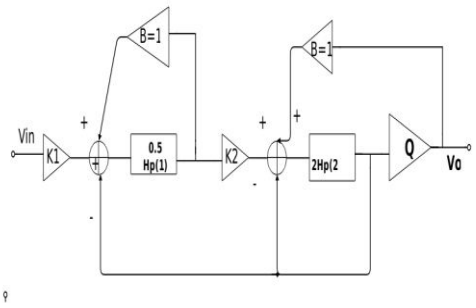
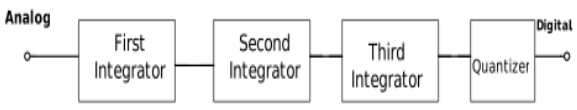


Fig 3. (b) Implementation with active-passive integrators

The conventional second-order architecture of Fig.3 (a) becomes the scheme of Fig.3 (b) with coefficients ½ and 2 incorporated in the Hp blocks. The value of K1 and K2 should be equal to $1/\alpha 1$ and $1/\alpha 2$, respectively, but the gain in the first integrator cannot be greater than 1 because it would alter the input dynamic range and the active stage would operate in a nonlinear region. The $\alpha 1$ attenuation can be compensated together with $\alpha 2$ but the resulting gain can become larger. A compromise solution is to accept some attenuation that, in sequence, reduces the SNR.

A. Third Order Active-Passive Delta Sigma modulator

An active-passive integrator in a second delta-sigma modulator possibly achieves excellent performance but the SNR reductions induced by variations in technology parameters can be problematic. Improving the SNR with higher OSRs give rise to quadratic increase in power in active blocks. Using additional passive integrator as the first stage adds a zero in the NTF and increases by one the order of the modulator. Using additional passive integrator as the first stage adds a zero in the NTF and increases by one the order of the modulator family. In order to make the solution beneficial, the new zero must be just inside the z-domain unity circle, and for this, a very low.



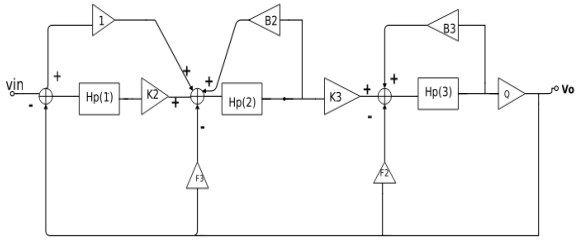


Fig 4 Block diagram of a Third Order delta-sigma modulator

Time constant equivalent RC network is needed. However, the passive integrator causes signal attenuation to be compensated with the gain block of successive stage. Fig 4 shows the behavioural diagram of the resulting third-order active-passive modulator. The scheme also uses a feed forward path, bringing the input signal to the input of second passive integrator, which corrects the position of the signal transfer function poles. Moreover, the output signal that feeds back to the input of the third passive integrator is attenuated (the factor F2 is less than1) to match the low swing at the output of the block K3. The transfer function from the input of the block Hp $(\boldsymbol{\alpha 1, z})$ to a node A (first summing point) is

$$HA(z) = \frac{\alpha 1K2\,z^{-1}}{[1-(1-\alpha 1)z^{-1}]} = \frac{\alpha 1K2z^{-1}}{[1-b1z^{-1}]} \text{ ------- (2).}$$

Where b1= [1-$\alpha 1$].The transform function from the input of block Hp $(\alpha 2, z)$ to node B (next summing point)

$$HB(z) = \frac{\alpha 2K3\,z^{-1}}{[1-Z^{-1}+\alpha 2(1-\beta 2)z^{-1}]} = \frac{\alpha 2K3\,z^{-1}}{[1-b2z^{-1}]} \text{------ -- (3).}$$

Where b2=$[1-\alpha 2(1-\beta 2)]$. The transform function from the input of block Hp $(\alpha 2, z)$ to node B (next takeoff point before quantizer)

$$Hc(z) = \frac{\alpha 2K3\,z^{-1}}{[1-Z^{-1}+\alpha 3(1-\beta 3)z^{-1}]} = \frac{\alpha 3z^{-1}}{[1-b3z^{-1}]} \text{--------- - (4).}$$

Where b3=$[1-\alpha 3(1-\beta 3)z^{-1}]$ all three transfer functions and the block diagram with linear quantizer gain of Fig.4 yield

$[\{Vin-Vo)HA + Vin - F1Vo\}HB - F2Vo]G\,HC + \in Q = Vo$

. This determines the STF and NTF

$$\text{STF (z)} = \frac{z^{-2}[1+\gamma z^{-1}]}{[1+\delta 1 z^{-1}+\delta 2 z^{-2}+\delta 3 z^{-3}}$$

$$\text{NTF (z)} = \frac{[1-\alpha 1 z^{-1}][1-\alpha 2 z^{-1}][1-\alpha 3 z^{-1}]}{[1+\delta 1 z^{-1}+\delta 2 z^{-2}+\delta 3 z^{-3}}$$

Where the γ, δ parameters depend on the modulator parameter. The task of the designer is to ensure ability and maximize the SNR for the chosen oversampling ratio. Indeed a third order architecture is not always stable when a single comparator is used. There is a complex dependence of the SNR on the design parameters and the optimal set can be determined by recursive behavioural simulations. The goal is to achieve a maximum SNR and minimum sensitivity due to a variation in parameters. According to the linear model of the quantizer, it is working as a gain stage with gain G. The equivalent gain G of the quantizer is defined as the ratio of its output root-mean-square (rms) value to its input rms value. Since delta-sigma modulator is a non linear system, this gain G can only be determined by simulation. The denominators denote three poles where the real is located at z=0.92/it is close to z=1 and reduces the benefit of the NTF by a factor of 1.25, and it is also affects the STF. However, the STF has a zero at z=0.865 that almost neutralizes the real pole. The complex conjugate poles of the denominators are at z=0.356 $\pm$ j 0.423, relatively far away from z=1.The zeros of the NTF are around z=1; the product of their distances from z=1 is 2.7×10^{-7}.The resulting NTF at z=1, accounting for the attenuation of all the poles, is -105dB.

$$\text{STF (z)} = \frac{z^{-2}(0.68-0.64z^{-1})}{[1-1.63z^{-1}+0.96z^{-2}-0.28z^{-3}]}$$

$$\text{NTF (z)} = \frac{[1-3.01z^{-1}+3.01z^{-2}-1.006z^{-3}]}{[1-1.63z^{-1}+0.96z^{-2}-0.28z^{-3}]}$$

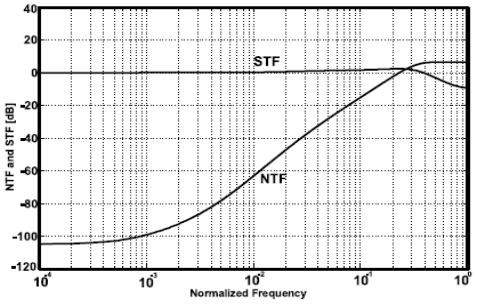


Fig5.STF and NTF of a modulator

IV. CIRCUIT IMPLEMENTATION OF SC INTEGRATOR

Fig 6 shows the SC implementation of second block of Fig.4.The schematic shown in Fig 2(b) realizes the active blocks. The external reference voltages are Vrep= 1.8 V, Vren = -1.8V, Vcm = Vcmfb = 1.8V. Capacitors with Cs=200pf and Ci=19.8pf.All the transistors in the design have aspect ratio of $9\mu m/0.18\mu m$.

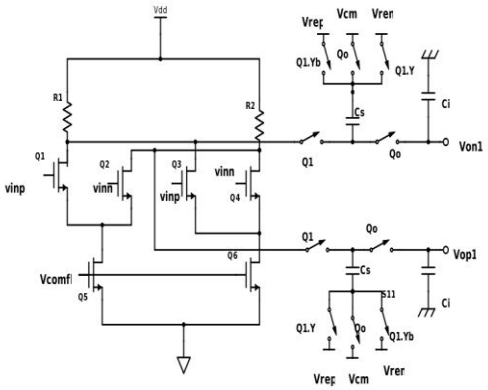


Fig.6. Fully differential implementation of Second integrator

The proposed design consists of two back-to-back connected differential amplifiers. It is used to add two currents there by acts as a built-in current adder. Output of current adder is given to SC integrator. This leads to reduction of signal swing at the output of integrator (because of passive components use SC integrator). It is compensated by amplifier of next (third) integrator.

Figure shows the switched capacitor circuit in a fully differential implementation. The sampling and feedback paths are separated to minimize the signal dependent charging and discharging from the signal and reference sources. Due to the voltage divider formed by two Cs, the input signal swing is reduced, and the modulator's performance is sacrificed. Bottom plate sampling is used to reduce signal dependent charge injection error. To limit the overall loop delay to a single clock cycle, Ci should sample from Cs during$\emptyset o$. vop1-von1 is basically the addition of the amplifier output and the data Y. In $\emptyset 1$ phase, the amplifier output is added (or equivalently subtracted) from the data and in $\emptyset o$ phase, the charge is transferred to the output. $\emptyset 1, \emptyset o$ $\emptyset 1.Y$ is the advanced version of $\emptyset 1$, $\emptyset 1$.Yb is the complement version of $\emptyset 1.Y$ .The

circuit that produce non-overlapping clock pulses is NAND latch.

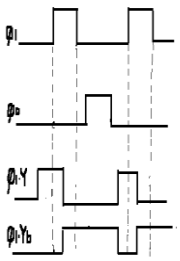


Fig.7. Non overlapping waveforms

A. Noise performance: The noise of first integrator dominates noise performance because of the noise of the later stages is suppressed by the gain of the preceding integrators. Therefore, the performance

depends on the KT/C power of the sampling capacitor divided by the oversampling ratio. If Cs is sampling capacitor of a fully differential scheme, the in band KT/C noise caused by the sampling capacitance Cs is

$$Vn^2=\frac{4kT}{Cs(OSR)}$$

Supposing that VFS is the full-scale voltage and $\bar{n}$ is the target bit, the value of Cs that gives rise to a nose voltage equal to half least-significant (LSB) is

$$Cs=\frac{4.k.T.2^{2n}}{(OSR)}$$

V. SIMULATION RESULTS

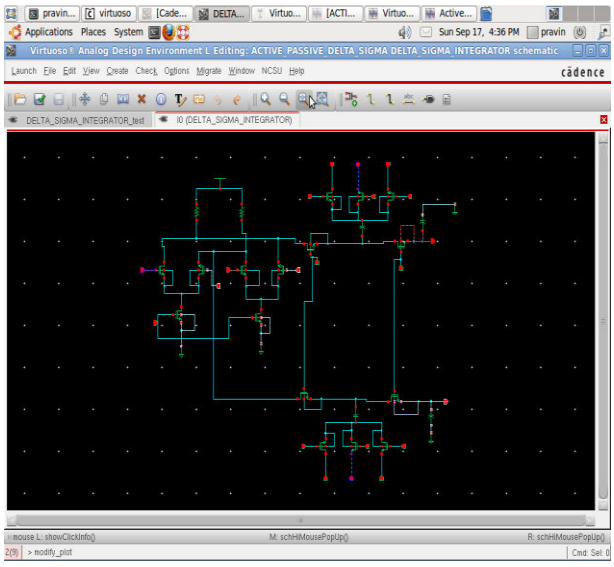


Fig. 8 (a) Designing Schematic of Second integrator

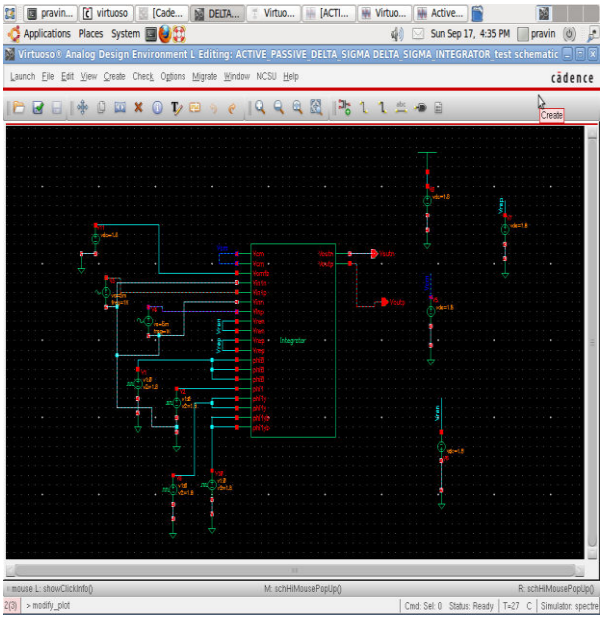


Fig 8. (b) Cell view of above schematic

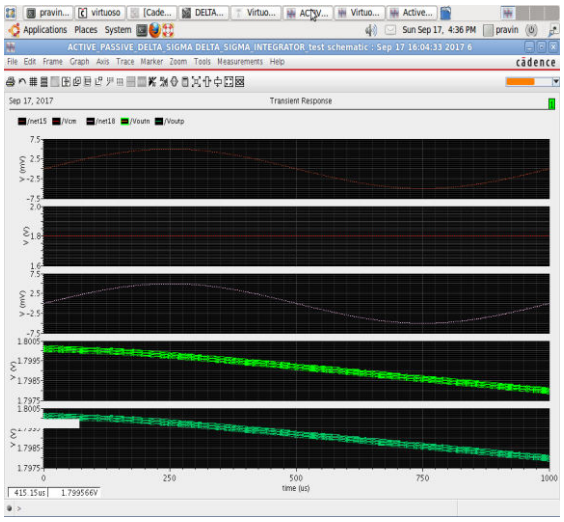


Fig.9 output waveforms

A. Power Calculations

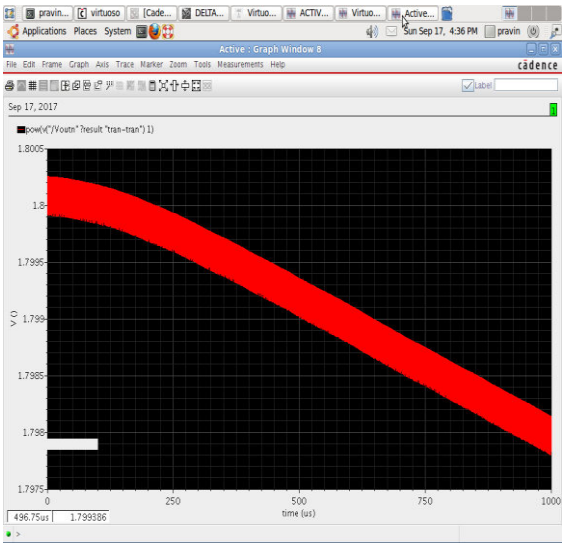


Fig.10.Graph of a power

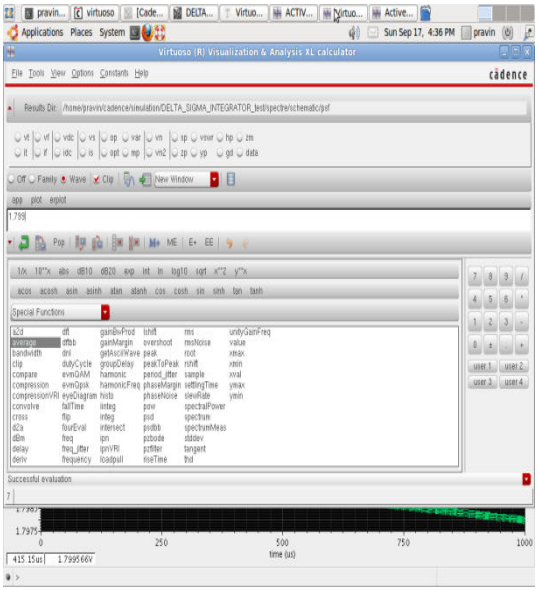


Fig. 11 power calculations

The measured modulator's power consumption is 1.79mW obtained from the simulation results using 180nm CMOS.

VI. CONCLUSION

A method utilizing a low gain amplifier with a positive feedback that improves the performance of a passive SC integrator and makes it suitable for use in high resolution delta-sigma modulator was introduced. The method significantly reduces the power consumed and achieves power effectiveness compare to conventional op-amp based SC integrator. The 180-nm CMOS prototype that uses a passive SC integrator achieves a power of 1.792mW for the supply voltage of 1.8 V.

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