Design and Implementation of S R Flip flop for Efficient power using CMOS 90nm Technology

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ABSTRACT

The main objective of this paper is to design SR flip-flop by using CMOS 90nm technology for efficient power. SR flip-flop is a sequential circuit. Three types of simulation will be performed in order to ensure that the implementation is fully functional. The SR flip-flop's schematic simulation using CMOS FET, layout model by using semi custom design technology and by using fully custom design technology are made. After performing the simulation, comparison is done between three layout auto generated, semicustom and fully custom on the basis of power and area.

Keywords: SR flip-flop, Sequential circuit, CMOS FET, layout, Power

I. INTRODUCTION

A sequential circuits, is one which the output is determined by the current inputs as well as the previously applied input variables. Such circuits said to have a state .Memory is used to store past values of states and outputs. Sequential circuits are usually designed with flip-flops or latches, which are sometimes called memory elements that hold data called tokens. Regenerative or sequential circuits are classified as bistable, mono stable and astable. Bistable states have two stable states or operation modes, each of which can be attained under certain input and output conditions. Among these main groups of regenerative circuit types, the bistable circuits are by far the most widely used and most important class. All basic latches flip-flops, registers and memory elements used in digital systems fall into this category. [2]

Very-large-scale integration (**VLSI**) is the process of creating an integrated circuit (IC) by combining thousands of transistors into a single chip. VLSI began in the 1970s when complex semiconductor and communication technologies were being developed. Before the introduction of VLSI technology, most ICs had a limited set of functions they could perform. ICs have three key advantages over digital circuits, size, speed and power consumption. A number of different IC fabrication technologies are available to us. The most important difference between technologies is the types of transistors they can produce[4]. MOSFETs offer the advantage that they draw almost zero control current while idle. They come in two flavours: pMOS and nMOS using n- and p-type dopants respectively. Even though an individual CMOS transistor uses very little energy each time it switches, the enormous number of transistors switching at very high rates of speed have made power consumption a major design consideration again. In this paper the performance estimation of SR flip-flop is done based on power measured.

II. SR FLIP-FLOP

The NAND-based SR latch can be implemented by gating the clock input, as shown in Fig. 1. Both the input signals S and R as well as the clock signal CK are active low. This means that the input signal will be ignored when the clock is equal to logic "1" and that inputs will influence the outputs only when the clock is active (i.e. CK="0"). For the circuit implementation of this clocked NAND-based SR latch, an OAI (OR-AND-INVERT) structure can be used, which is analogous to the AOI-based realization of the clocked NOR SR latch.

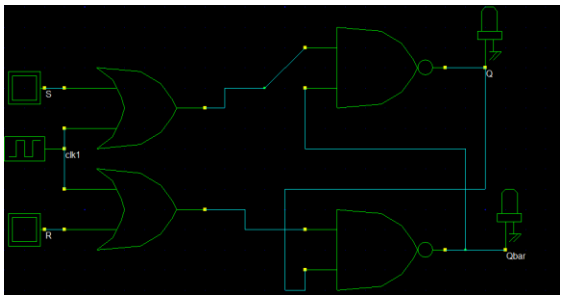

Fig.1. Gate-level schematic of the clocked NAND-based SR latch circuit, with active low inputs.

The SR flip-flop truth table is shown in Table 1.

Table 1

When CK = 1, S' = R' =1 independent of the values of S and R => HOLD

	CK	S	R	Q_{n+1}	$\overline{Q}_{n+1}$	Operation	
"ACTIVE LOW"	0	0	0	0	0	NOT allowed	S' = R' = 0
	0	0	1	1	0	set	
	0	1	0	0	1	reset	
	1	x	x	Q_n	$\overline{Q}_n$	hold	

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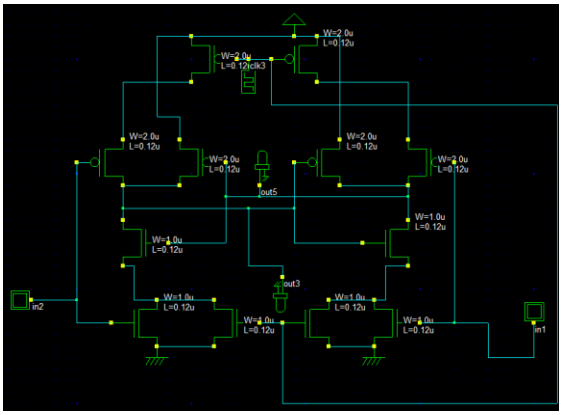


Fig.2. AOI (AND-OR-INVERT)-based implementation of the clocked NOR-based SR latch circuit

III. LAYOUT DESIGN SIMULATION

In first method the schematic of SR flip-flop is designed. Using Microwind software the auto generated layout of SR flip-flop is created, and then simulate the layout. In this paper 90nm foundary is selected. The figure 3 represents this auto generated layout.

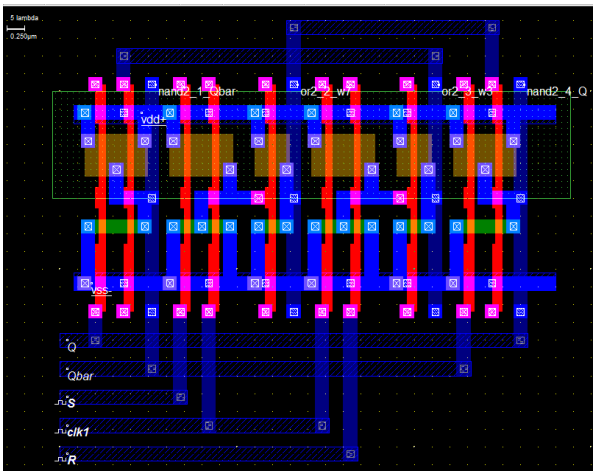


Fig. 3. Auto generated SR flp-flop

This layout is checked for DRC if there is no error then it is simulated. And generated timing waveforms are verified on comparing to the circuit operation. The power is measured by the simulation result. The figure 4 shows the timing diagram of this automatic layout.

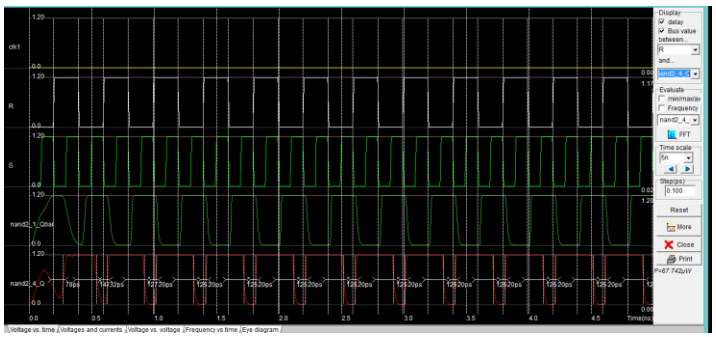


Fig.4. Timing Diagram of Automatic Generated Layout

We measure the power consuming by this layout and from the properties of layout area is measured. Here the consuming power is 67.742 µWatt. Area required for this particular layout is45.3µm^2 .Width is 7.3 µm and height is 6.2 µm.

In second step we prepare layout using semicustom approach. In semicustom approach transistors are in-bult. In this approach connections are made by the developer following lambda design rules. There is possibility of power reduction.

Figure 5 represents the layout using semicustom approach.

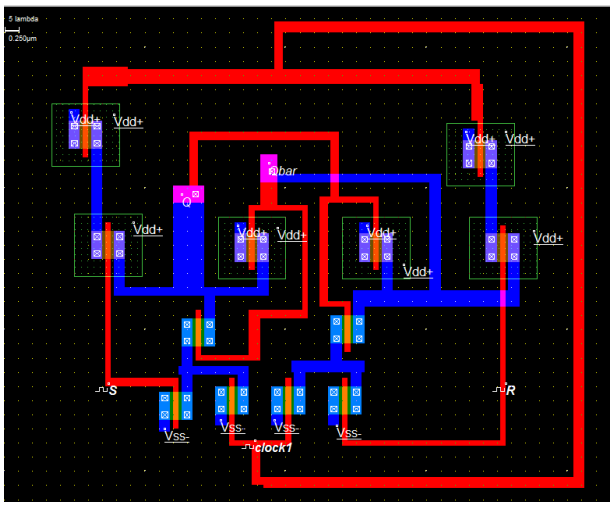


Fig. 5. Semi custom Layout of SR flip-flop

The semicustom layout is checked for DRC if there is no error present in layout, the circuit is simulated and timing waveforms are generated. The generated timing waveforms are verified with the truth table or operation of original circuit. Figure 6 shows the timing diagram of semicustom layout.

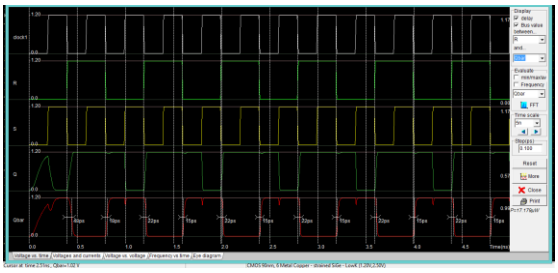


Fig.6. Timing Diagram of Semi custom layout

The power is observed from this particular simulation. Here power is 17.179 µWatt, less than automatic layout. And area is calculated from the properties. Here the width is 9.5 µm (181 lambda) and height is 8.3 µm (165 lambda). In semicustom layout area is 78 μm^2.
In third step fully custom approach is used. **Full-custom** design is a methodology for designing integrated circuits by specifying the layout of each individual transistor and the interconnections between the Full-custom design potentially maximizes the performance of the chip, and minimizes its area, but is extremely labor-intensive to implement.

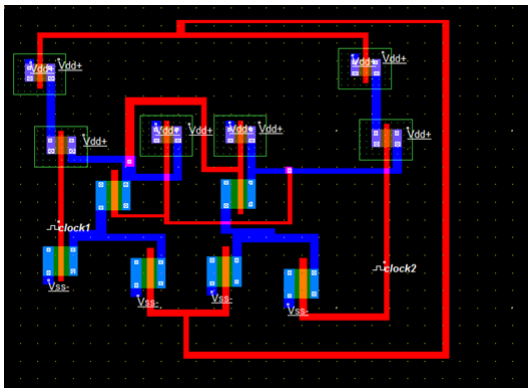


Fig.6. Full custom layout of SR flip flop

Measured width 7.7 (219- lambda) µm and 8.6µm (245-lambda). Measured area is 65 μm^2.Power is again reduced Created layout is checked for DRC and simulate. The timing waveforms are verified with original circuit operation. Power is measured from this simulation. In full custom design approach there is high power reduction but some amount of area is incremented. In this layout power consumed is 8µWatt. Figure 7 shows the timing diagram of this fully customized circuit.

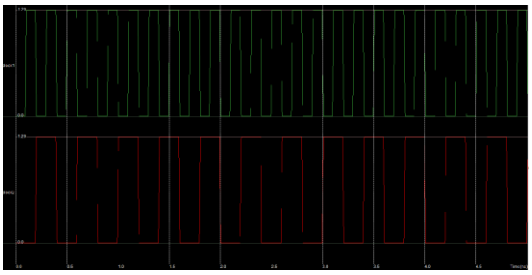


Fig.6. Timing Diagram of Full custom layout

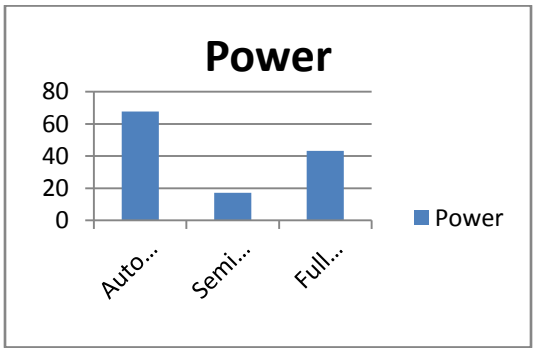
IV. RESULT COMPARISON

The performance of proposed full subtractor layout is compared with semicustom approach as well as automated layout. The performance parameters are Area and Power. From above results a comparative study can be done between three designing approaches. Table 3 shows comparative analysis.

Table 3: Comparative Analysis For Area And Power

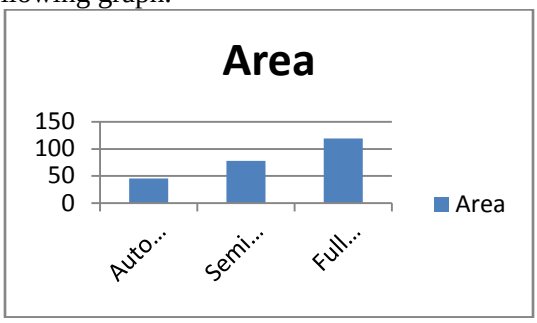
Approach	Area (μm^2)	Power (µWatt)
Auto generated	45.3	67.742
Semi - custom	78	17.179
Full - custom	119	43.184

Comparative analysis table shows that in terms of power the performance of automatic layout approach increases. In terms of area the full custom layout has better performance among three design approaches.
Power graph of these three design approaches is shown below:



From the above graph we observed, there is a reduction of 75% in power for semi custom with auto generated layout. And there is 39% reduction in power with full custom layout. Performance is increases in terms of power required. This fully customized layout is used in compact size applications.

But more area is required in full custom approach. Comparative analysis in terms of area is done through the following graph.



From above graph it is observed that fully customized layouts have more area than semi customized and auto generated.

V. CONCLUSION

From the above result analysis it is clear that the fully customized layout is more efficient in terms of power. Fully customized layout is 39% is better than semi custom layout and 75% is better than auto generated layout approaches. So this design approach can be implemented where power reduction is the main consideration. In this approach area compensates for power.

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