Design Of Ultra Low Power Vedic Multiplier using Adiabatic Logic

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Abstract— Low power circuit designs have been an important issue VLSI design areas. Multipliers play a major role in high performance systems. Vedic mathematics is world renowned for its algorithms that yield quicker results, be it for mental calculations or hardware design. The Urdhva-Tiryagbyham Vedic multiplier is one such multiplier which is effective both in terms of speed and power. Adiabatic logic style is said to be an attractive solution for low power electronic applications. By using Adiabatic techniques energy dissipation in PMOS network can be minimized and some of energy stored at load capacitance can be recycled instead of dissipated as heat. In analysis, two logic families, ECRL (Efficient Charge Recovery Logic) and PFAL (Positive Feedback Adiabatic Logic) are compared with EEAL(Energy Efficient Adiabatic Logic) for Vedic multiplier circuits. Tanner EDA tools are used for simulation.

Keywords—Low-power, Adiabatic Logic, Vedic multiplier.

I. INTRODUCTION

Multipliers play an important role in computation and other advanced mechanism, which makes them one of the key components of every ALU. Multiplication, requires substantially more hard-ware resources and processing time than addition and subtraction. The need of high speed multiplier is increasing as the need of high speed processors are increasing. Higher throughput arithmetic operations are important to achieve the desired performance in many real time signal and image processing applications. Vedic mathematics is the name given to the ancient system of mathematics, which was rediscovered from the ancient Indian scriptures between 1911 and 1918 by Jagadguru Swami Sri Bharati Krisna Tirthaji (1884-1960), a scholar of Sanskrit, mathematics, history and philosophy. The whole of Vedic mathematics is based on 16 Vedic sutras, which are actually word formulae describing natural ways of solving a whole range of mathematical problems. The term “adiabatic” describe the thermodynamic processes in which no energy exchange with the environment, and therefore no dissipated energy loss. Adiabatic circuits are those circuits which work on the principle of adiabatic charging and discharging and which recycle energy from output nodes instead of discharging it to ground.

II. RELATED WORKS

Abhijit Asati .et al[2] enforced the associate in nursing improved high speed, totally pipelined eight.8 signed Baugh Wooley number circuit has been designed and enforced mistreatment CMOS TSPC logic in zero.6μm, N-well CMOS method of MOSIS utilizing optimized TSPC logic cells. By planning and mistreatment novel TSPC full adder cell, Baugh Wooley number implementation had massive reduction in junction transistor count, average power and delay. The full junction transistor count, average power and most instant power are analyzed. Chanda M. et al [3] enforced ordered logic circuits by employing a novel Quasi-Static Single-phase adiabatic Dynamic Logic (SPADL). SPADL uses solely one curving supply as supply-clock. It considerably decreases circuit complexness with improved driving ability gate lustiness. A sensible adiabatic asynchronous ordered circuit supported the energy economical SPADL is enforced with TSMC zero.18μm technology.

Gang Chow dynasty et al.[5] delineate complexness analysis [both in application-specific integrated circuits (ASICs) and on field-programmable gate arrays (FPGAs)] and economical FPGA implementations of bit parallel mixed Karatsuba–Ofman Multipliers (KOM). The analysis is extended by mistreatment 4-input/6-input search tables (LUT) on FPGAs.

Hadi Parandeh-Afshar et al [6] improved the performance of FPGA for carry save arithmetic. In addition to multiplication and multiply accumulation, the FPCA will accelerate additional general carry-save operations, like multi-input addition and multipliers that are united with different adders.
Himanshu Thapliyal designed [15] associate in nursing economical methodology of Elliptic Curve coding mistreatment Ancient Indian religious writing arithmetic. Economical hardware electronic equipment for purpose doubling uses sq. algorithms of Ancient Indian religious writing arithmetic. so as to calculate the sq. of variety, “Duplex” D property of binary range is employed.

Paramasivam M.E. et al [10] designed associate in nursing economical Bit Reduction Binary Multiplication algorithmic program mistreatment religious writing strategies. The work in the main focuses on speed of the multiplication operation of multipliers, by reducing the amount of bits to be increased. The framework of the planned algorithmic program is taken from Mathematical algorithms given in Vedas and is any optimized by use of some general arithmetic operations like enlargement and bit-shifting.

Partha Pratim Kundu. et al [9] designed a Wallace Tree number for DSP applications. In this paper a completely unique technique to see the optimum module set has been introduced associate in nursing an economical RNS number supported Wallace Tree number (for thirty two bit arithmetic unit) for DSP applications.

Saha D. et al [1] designed Energy economical adiabatic Logic (EEAL) could be a dual-rail adiabatic logic that consists of 2 DCVS network and a combine of cross-coupled PMOS devices in every stage. It needs only 1 curving power provide, has straightforward implementation, and performs higher than the antecedently planned adiabatic logic families in terms of energy consumption. As single clock circuit needs straightforward clock theme, this logic vogue will relish least management overheads. Forward the complementary output nodes (“out” and “outb”) ar ab initio low and provide clock ramps up from logic zero to (“0”) to logic 1(“VDD”) state. currently if “in”=“0” and inb=“1” N1, money supply are turned off and M2,N2 and P1 are turned ON. The OUT node is then charged by following power provide clock closely through the parallel combination of PMOS (P1) and NMOS (M2), whereas “outb” potential is unbroken at ground potential, as N2 is ON. Once the availability clock swings from “VDD” to ground, “out” Node is discharged through an equivalent charging path and un-driven “outb” is unbroken at ground potential. Resultantly full swing are often obtained in “out” node and ground potential at “outb” node. The power consumed by this EEAL logic is considerably reduced than the opposite standard multipliers.

Yasuhiro Takahashi [16] designed of a 16-bit computer architecture processor core mistreatment associate in nursing adiabatic logic that is termed a 2 section drive adiabatic dynamic CMOS logic (2PADCL). adiabatic computer architecture processor is non-pipelined with a latency of 3 cycles, Associate in Nursing additionally consists of six blocks; an arithmetic and logic unit (ALU), a program counter, a register, associate in nursing instruction decoder unit, a electronic device and a clock management unit.

III. VEDIC MULTIPLICATION

‘Vedic’ is term derived from the word ‘Veda’, which means storehouse of all knowledge. Vedic mathematics logics and steps have applied to problem involving trigonometric functions, Plane and sphere geometry, applied mathematics conics, differential calculus and integral calculus and of different kind. This has attributed to fact that the Vedic formulae have claimed to be building on natural principles on which human mind works. Thus, this shows some efficient algorithms, which can apply to various branches of applied science.

A. Urdhva-Tiryagbhyam Sutra

The proposed Vedic multiplier is based on the “Urdhva Tiryagbhyam” sutra (algorithm). Urdhva-Tiryagbhyam sutra which is the general formula applicable to all cases of multiplication and will also be found very useful in the division of a large number by another large number. The formula itself is very short and terse, consisting of only one compound word and means “vertically and cross-wise”. Urdhva” and “Tiryagbhyam” words are derived from Sanskrit literature. Urdhva means “Vertically” and Tiryagbhyam means “crosswise”. It is based on a novel concept, where the generation of all partial products can be done with the concurrent addition of partial products.

To illustrate this scheme, let us consider the multiplication of two decimal numbers 252 x 846 by Urdhva-Tiryagbhyam method as shown in fig 1. The digits on the both sides of the line are multiplied and added with the carry from the previous step. This generates one of the bits of the result and a carry. This carry is added in the next step and hence the process goes on. If more than one line are there in one step, all the results are added to the previous carry. In each step, least significant bit acts as the result bit and all other bits act as carry for the next step. Initially the carry is taken to be zero.
IV. EFFICIENT CHARGE– RECOVERY LOGIC (ECRL)

Efficient Charge – Recovery Logic (ECRL) uses cross-coupled PMOS transistors. It’s the structure kind of like Cascode Voltage Switch Logic (CVSL) with differential sign. It consists of 2 cross-coupled transistors money supply and money supply and 2 NMOS transistors within the N-functional blocks for the ECRL adiabatic logic block. An AC power provide PWR is employed for ECRL gates, therefore on recover and recycle the equipped energy. Each out and I_{out} square measure generated in order that the ability clock generator will perpetually drive a continuing load capacitance freelance of the input. Full output swing is obtained as a result of the cross-coupled PMOS transistors in each pre-charge and recovers phases. However attributable to the brink voltage of the PMOS transistors, the circuits suffer from the non-adiabatic loss each within the pre-charge and recover phases. That is, to say, ECRL perpetually pumps charge on the output with a full swing. However, because the voltage on the provision clock approaches to V_{tp}, the PMOS electronic transistor gets turned off.

So the recovery path to the provision clock is disconnected, thus, leading to incomplete recovery. V_{tp} is that the threshold voltage of PMOS semiconductor device. The number of loss is given as

\[ \text{EECRL} = C|V_{tp}|^2 / a \text{ pair of} \]

It may be inferred that the non-adiabatic energy loss depends on the load capacitance and freelance of the frequency of operation. The ECRL circuit’s area unit operated during a pipelining vogue with the four-phase provides clocks. Once the output is directly connected to the input of ensuing stage (which could be a combinatory logic), just one part is enough for a logic price to propagate. However, once the output of a gate is fed back to the input, the provision clocks ought to be in part. A latch is one in all the best cases that have a feedback path. The input signals propagate to ensuing stage during a single part, and also the input values area unit holds on in four phases (1-clock) safely. Allow us to assume in is at high and in b is at low. At the start of a cycle, once the provision clock ‘pwr’ rises from zero to V_{dd}, out remains at a ground level, as result of in activates F-tree (NMOS logic tree). I out follows water-cooled reactor through money supply. When power reaches V_{dd} the outputs hold valid logic levels. These values area unit maintained throughout the hold part and used as inputs for the analysis of ensuing stage. When the hold part, water-cooled reactor falls right down to a ground level, /out node returns its energy to water-cooled reactor so the delivered charge is recovered. Thus, the clock water-cooled reactor acts as each a clock and power provide. A major disadvantage of this circuit is that the existence of the coupling effects, as a result of two outputs area unit connected by the PMOS latch and also the two complementary outputs will interfere one another.

V. POSITIVE FEEDBACK ADIABATIC LOGIC (PFAL)

The partial energy recovery circuit structure named feedback adiabatic Logic (PFAL) has been used, since it shows very cheap energy consumption if compared to alternative similar families, and an honest strength against technological parameter variations. It’s a dual-rail circuit with partial energy recovery.

The core of all the PFAL gates is associate adiabatic electronic equipment, a latch created by two PMOS M1-M2 and two NMOS M3-M4, that
avoids a logic level degradation on the output nodes out and /out. The 2 n-trees notice the logic functions. This logic family conjointly generates each positive and negative output. The useful blocks area unit in parallel with the PMOSFETs of the adiabatic electronic equipment and type a transmission gate. The two n-trees notice the logic functions.

Two major variations with relevancy in ECRL area unit that the latch is formed by two PMOSFETs and two NMOSFETS, instead of by solely two PMOSFETs as in ECRL logic, which the useful blocks area unit in parallel with the transmission PMOSFETs. So the equivalent resistance is smaller once the capacitance must be charged.

PFAL uses a four-phase power-clock water-cooled reactor $\phi(t)$. $\phi(t)$ rises from zero to $V_{dd}$ within the appraise section (E) and provides energy to the circuit, then $\phi(t)$ returns to zero within the RECOVERY section (R) and also the energy flows back from the circuit to the power-clock generator; the HOLD section (H) and also the IDLE section (I) are required for cascading gates.

VI. GENERAL VEDIC MULTIPLIER STRUCTURE

The method is explained below two 2 bit numbers A and B wherever $A = a1a0$ and $B = b1b0$ as shown in Fig. Firstly, the smallest amount vital bits area unit increased which supply the smallest amount vital little bit of the ultimate product (vertical). Then, the LSB of the number is increased with following higher little bit of the number and additional with, the merchandise of LSB of number and next higher little bit of the number (crosswise). The add offers second little bit of the ultimate product and also the carry is additional with the partial product obtained by multiplying the foremost vital bits to relinquish the add and carry. The add is that the third corresponding bit and carry becomes the fourth little bit of the ultimate product. This multiplication technique is applicable for all the cases. The Vedic Multiplication technique for two 2-bit Binary Numbers

\[
\begin{array}{cccc}
  a_1 & a_0 & a_1 & a_0 \\
  b_1 & b_0 & b_1 & b_0 \\
\end{array}
\]

Fig 4. Vedic Multiplication of 2-bit binary number

The 2X2 Vedic number module is enforced mistreatment four input AND gates & two half-adders that is displayed in its diagram in Fig. it's found that the hardware design of 2x2 bit Vedic number is same because the hardware design of 2x2 bit standard Array number. Thence it's complete that multiplication of two bit binary numbers by Vedic technique doesn't created vital result in improvement of the multiplier’s potency. Terribly exactly we are able to state that the entire delay is merely 2-half adder delays, when final bit product area unit generated, that is incredibly almost like Array number. By using this 2*2 multiplier block 4*4,8*8,16*16 etc multiplier block can be implemented. In N*N multiplication we need four N/2*N/2 multipliers, two N bit Adders, a half adder and a N/2 bit adder.

VII. RESULTS AND SIMULATIONS

![Diagram of Vedic Multiplier](image-url)
During simulation we have to apply \{A\} and \{B\} as inputs. The simulated waveform of 8x8 Adiabatic Vedic multiplier as shown in Fig. The output waveform for ECRL and PFAL adiabatic logic is given below. Then the comparison table for the power and delay factor is given.

Fig 6. Schematic Architecture for 8x8 Vedic multiplier

Fig 7. Schematic of 4x4 Vedic multiplier

Figure 7. Simulation waveform of ECRL

Figure 8. Simulation Waveform of PFAL
A new adiabatic multiplier structure based on Urdhva Triyakbhyam sutra of Vedic mathematics has been proposed using ECRL and PFAL style. It can be concluded that the power and delay of the proposed adiabatic logic is significantly reduced than other logic styles such as existing EEAL logic based multiplier. The simulation and the schematic verification can be done in TANNER EDA. This could be an efficient power related circuit for the future IC’S.

REFERENCES


